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Analysis, design and implementation of a generalized step-up/step-down solid state transformer using PWM switching

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ANALYSIS, DESIGN AND IMPLEMENTATION OF A GENERALIZED STEP-UP/STEP-DOWN SOLID STATE TRANSFORMER USING PWM SWITCHING

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ABSTRACT

ANALYSIS, DESIGN AND IMPLEMENTATION OF A GENERALIZED STEP-UP/STEP-DOWN SOLID STATE TRANSFORMER USING PWM SWITCHING

by Usamah S. Hassan

The solid state transformer has many advantages over the conventional transformer, the most important of which is superior line and load regulation under transient conditions and an electronically adjustable turns ratio.

The solid state transformer is based on Buck-Boost converter topology and uses pulse width modulation (PWM) switch-mode technology. The solid state transformer accepts alternating current (AC) input voltage and delivers regulated AC output voltage by using bi-directional switches so that the transformer achieves bi-directional energy transfer. It is also capable of step-up/step-down performance. Theoretical analysis and control loop design are presented. A prototype solid state transformer was implemented for 1kW power performance. Experimental results of the transformer and hardware implementation issues are also discussed and promise the advantages of line and load regulation in the closed loop system.

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1. INTRODUCTION

1.1 Overview

This project looks at the available topologies of solid state alternating current (AC) chopper converters employing pulse width modulation (PWM) and other techniques. The different topologies are critically studied and compared to choose the best suitable topology for use in the solid state transformer. The design objective will be moderate power in the 1 kW range and a transformer with a programmable "turns ratio" that has a bi-directional energy flow.

The goal of this project is to replace electrical power transformers with solid state transformers that have the following advantages:

- Smaller size, less weight.
- Statically and dynamically adjustable turns ratio.
- Ability to provide line and load voltage regulation.
- Suppress transients that may be present on the input line.
- Maintain high efficiencies at reduced loads.
- Comparable operation to the auto transformer.

The main disadvantage of the solid state transformer at this time is that it does not provide electrical isolation between input and output terminals.

The solid state transformer accepts AC input voltage and delivers regulated AC output voltage as a ratio of the input line voltage. The generalized solid state transformer

can step-up or step-down the input voltage. It uses the Buck-Boost converter topology in which the switches are replaced by bi-directional switches to allow for AC operation and bi-directional energy transfer.

The block diagram of the generalized solid state transformer is shown in Figure 1.1. The system consists of the Buck-Boost converter with bi-directional switches and a feedback loop. The feedback path employs an output voltage attenuator, a comparator, a phase detector, a compensator, a duty cycle limiter, and a duty cycle generator (PWM) to drive the switches.

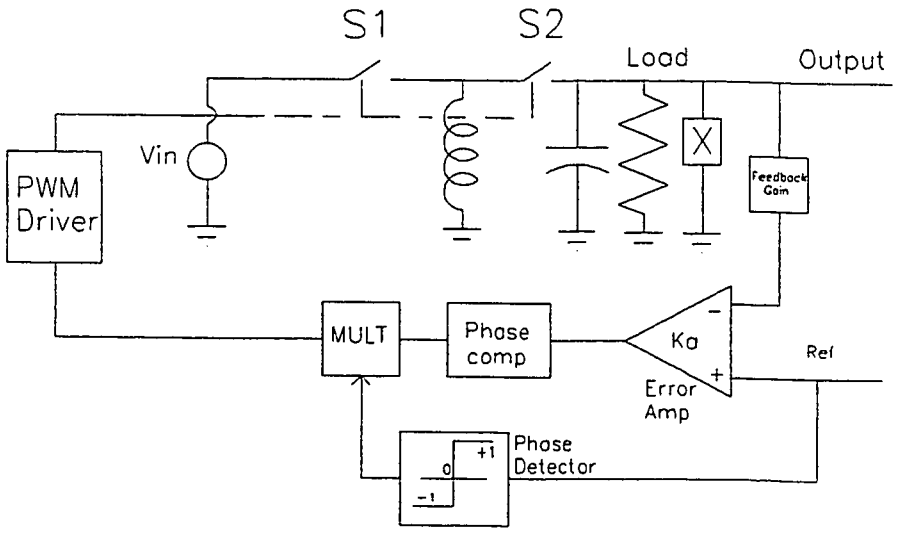

Figure 1-1: Solid state transformer block diagram showing different components of the system. Based on the Buck-Boost converter, it uses PWM driver circuits and feedback loop comparison and phase detection and compensation to provide closed-loop response.

1.2 Principle of Operation

The inductor in the Buck-Boost converter charges during the ON time of the S1 switch and reaches a maximum value. Energy is transferred from the input and stored in the inductor. Energy is then transferred from the inductor to the output capacitor and load during the OFF time of the S1 switch and ON time of the S2 switch. If for any reason the voltage is different, the feedback loop comes into action. The output voltage is attenuated and compared to a reference voltage. Since the Buck-Boost converter reverses the output voltage with respect to the input, the phase detector system detects the phase of the output voltage and maintains negative feedback at all times. The error signal output from the comparator is then fed to a PWM generator to convert it to a pulse train used turn on and turn off the S1 and S2 switches.

The duty cycle of the PWM is directly proportional to the error signal generated by the comparator and controls the ON-OFF states of the S1 and S2 switches, which control the amount of energy transferred to the output and dictates the output voltage. This method of control is called direct duty cycle control. There are other methods of control such as current mode control, which introduces the inductor current as a feedback parameter. Details of direct duty cycle control and current mode control are discussed in Chapter 4.

2. LITERATURE REVIEW

2.1 The Beginnings of the Solid State Transformer

In a 1980 study conducted for the U.S. Navy, Bowers, Garret, Nienhaus, and Brooks (ref. 1) demonstrated by analysis and simulation the concept of a solid state transformer. Their transformer provided AC output regulation and used PWM AC switching technology. This was the beginning of the idea of a solid state transformer.

The solid state transformer was sought to achieve advantages such as:

- Smaller size, less weight.
- Statically and dynamically adjustable turns ratio.
- Ability to provide output regulation.
- Tendency to suppress input line transients.
- Alleviate need for the use of very large inductive components.
- High efficiency at reduced load. The conventional transformer has decreased efficiency at reduced loads because of core losses.

The solid state transformer in its present form has the disadvantage of the absence of electrical isolation between input and output. The original transformer design is based on the Buck-Boost DC to DC converter and is shown in Figure 2-1. It is comparable to an auto transformer except that the variable output voltage control is obtained by a potentiometer operating at low power levels in the feedback loop.

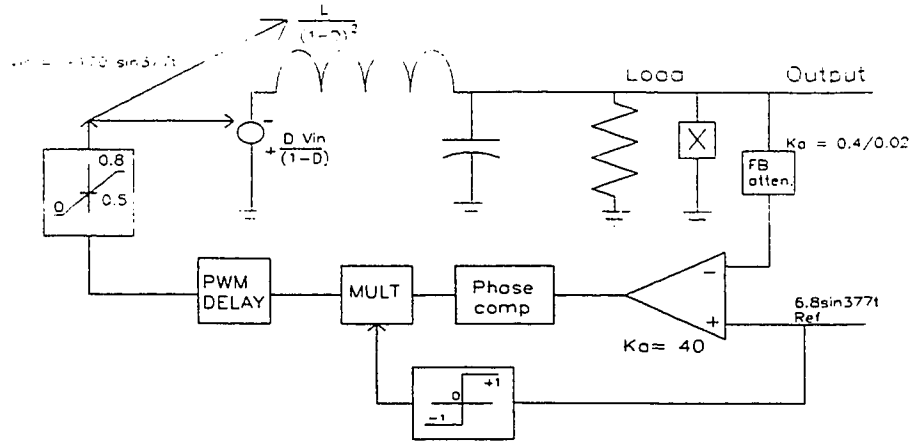

Figure 2-1: Solid state transformer (ref. 1). The transformer consists of the Buck-Boost converter in its averaged-state representation, duty cycle limiter, feedback attenuator, phase detection, and compensation.

Bowers, Garret, Nienhaus, and Brooks proposed analysis methods, adopted the widely used state space averaging method, and proposed the use of bi-directional switches to handle AC voltages. The converter is capable of stepping-up and stepping-down voltages depending on the value of the duty cycle (D). D is determined by the feedback attenuator and the amplitude of the reference voltage. If D is greater than 0.5, the converter boosts the input voltage, and if D is less than 0.5 it bucks the input voltage.

Special consideration must be taken because the Buck-Boost has the following characteristics:

- Output voltage is 180 degrees out of phase with the input voltage, resulting in added voltage stresses on the switches.

- Open-loop gain and low-pass filter transfer function are functions of D, which make it difficult to optimize system performance.

The design components were L = 25 uH, C = 100 uF to provide a high degree of attenuation to the 50 kHz chopper frequency and no significant attenuation to the 60 Hz input frequency. The design considered two extremes of operation:

- Maximum power at $V_o = 240V$, therefore $D = \frac{2}{3}$ and R = 48 Ohms.
- Maximum current $V_o = 12V$, therefore $D = \frac{1}{11}$ and R = 1 Ohm.

The circuit performance was monitored at these extremes and was assumed to work in between them. Because of stability considerations and differences between the open-loop DC gains at the two extremes, the gain adjustments were chosen to be in the feedback attenuator rather than in the automatic gain control (AGC) circuit, which generates the input reference signal. The circuit in Figure 2-1 consists of the following building blocks:

- State-space average model of the converter.
- Single pole approximation used for the PWM.
- Lead compensator for stability.
- Duty cycle limiter to limit the duty cycle to 0.8.
- Phase detector and multiplier to maintain negative feedback at all times.
- Comparator for error signal generation
- Adjustable feedback attenuator.

The results of Bowers, Garret, Nienhaus, and Brooks' study were verified only by computer simulation and were promising. The resultant system provided regulation at 1%. The simulation at the two extremes showed that the output voltage followed the input voltage closely. Bowers, Garret, Nienhaus, and Brooks concluded that, because of the unavailability of switches that can handle the stresses, a 0 to 2 step-up/step-down transformer could not be realized. This is quite achievable now with the advances in semiconductor devices and the introduction of high-power metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT) devices.

Bowers, Garret, Nienhaus, and Brooks' study did not recommend a transformer that offered combined step-up and step-down capabilities. This was because the phase reversal in the Buck-Boost severely increased the voltage stresses on the power switches. This is not a valid point today because of the availability of devices on the market that can withstand these voltage stresses. Snubbing circuits can also be designed to decrease these stresses. The main drawback of Bowers, Garret, Nienhaus, and Brooks' study is that it has not taken into account, in the model representation, the effect of parasitic capacitor equivalent series resistance (ESR). ESR accounts for an additional zero in the left-hand plane (in addition to the right-half plane zero) and can severely alter the stability of the circuit. If these parasitics (which inevitably exist in any practical circuit) are taken into account, the design of the stabilizing compensator needs to be altered. Nevertheless, Bowers, Garret, Nienhaus, and Brooks' study was one of the milestones in the realization of a solid state transformer because it considered all the pertinent issues of the design.

2.2 Design of a Novel AC Regulator

Lee, Yu, and Mahmoud (ref. 2) designed a regulator connected in series with the AC mains. In general, regulators are of four types:

- Adjustable mains transformers driven by motors.
- Electronically controlled tappings transformers.
- Saturable reactor regulators.
- AC⇒DC ⇒AC conversion regulators.

The first three types have the disadvantage of using bulky transformers. The fourth type has low efficiency and unidirectional power flow.

Lee, Yu, and Mahmoud's design develops an AC⇒AC electronic transformer that allows bi-directional flow of energy and produces incremental voltage changes. This represents an implementation of a solid state transformer. The design resulted in a 50W regulator with an efficiency of 96%. Lee, Yu, and Mahmoud's design is based on the Cuk converter that used a high-frequency transformer with a 1:1 turns ratio. The analysis of the circuit is performed using the state space averaging technique. The bode plot of output voltage change versus duty cycle change shows stable performance and acceptable phase and gain margins. Because transfer functions are different for different values of input voltage and duty cycle, the design was based on the worst case. The circuit parameters of the design (Figure 2-2) were as follows:

- Input 50 Hz signal was allowed in the range 43V to 83V root mean square (RMS).

- The output resistance R_o was allowed in the range of 150 Ohms to open circuit.
- The sampling frequency F_s was equal to 50 kHz.

The circuit measurements show that an input voltage change from 71V to 112V yielded an overshoot in the first half cycle of output voltage V_o. Changes in the output resistance R_L from 150 Ohms to infinity did not change V_o. The load of a nonlinear bridge, a 50μf capacitor, and an output resistance R_L of 150 Ohms connected in parallel with the capacitor yielded a slightly distorted V_o waveform.

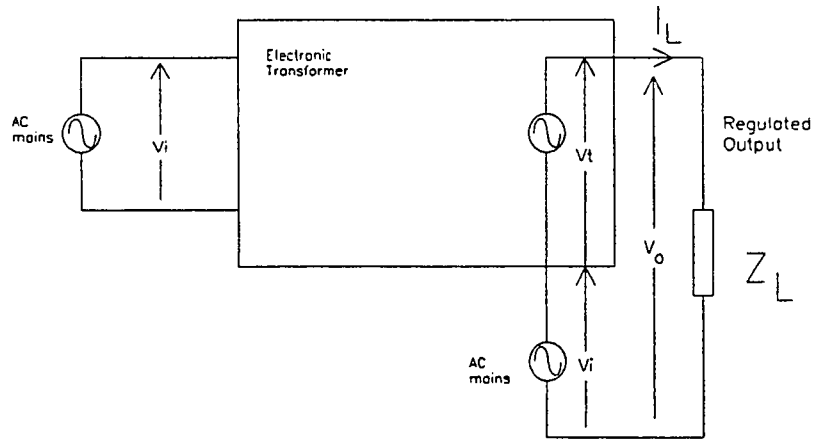

Figure 2-2: Novel AC regulator (ref. 2). The regulator consists of the electronic transformer that produces the incremental output V_t which is added to the input voltage V_i to produce the regulated output voltage V_o.

Although Lee, Yu, and Mahmoud's circuit demonstrated acceptable performance, it was unable to produce a voltage less than the maximum input voltage. Therefore, output voltage had to be less than or equal to the maximum input voltage. Subsequently, the

design could not be used to buck the input voltage, or be used as a combined electronic step-up/step-down transformer.

2.3 Single-Phase Sinusoidal Rectifier with Step-Up/Step-Down Characteristics

Itoh and Ishizaka (ref. 3) offered another implementation of the electronic solid state transformer. Their design replaced the single phase diode bridge coupled with a capacitor at the output terminal because this configuration had problems associated with current distortion and low power factor (PF). Their design was intended to be used in conjunction with the rectifier and inverter AC⇒DC⇒AC conversion system. Also, it performed the AC⇒DC conversion with step-up and step-down. When a constant voltage is used as an input for the inverter stage, the output waveform is distorted and PWM is merely for output regulation. However, when a rectifier and a converter of this type are used, the output voltage can be sinusoidal wave shaped. Two configurations can be realized based on Cuk and single-ended primary inductor (SEPIC) derived converters.

By using a current reference hysteresis control, the supply current is sinusoidal-wave-shaped with a near unity power factor. Voltage and current control is implemented by using a proportional plus integral plus derivative (PID) controller. Itoh and Ishizaka analyzed their design using the state space averaging method where the RMS of each variable is introduced. All the equations of the Cuk derived converter can be used. Experimental results were given at $\lambda = 1.5$ (conversion ratio). The response when varying the voltage reference was acceptable. The transient response when varying the load resistance looked acceptable and did not exhibit any wild oscillations or instability.

Nevertheless, Itoh and Ishizaka's design did not consider the AC⇒AC conversion case as opposed to AC⇒DC⇒AC (or the rectifier followed by an inverter case). They failed to address any of the control and stability issues when the duty ratio is varied. Furthermore, they did not address the possibility of an inductive or capacitive load, which needs to be taken into account to properly design the feedback-loop portion of the closed-loop system. The converter is shown in Figure 2-3.

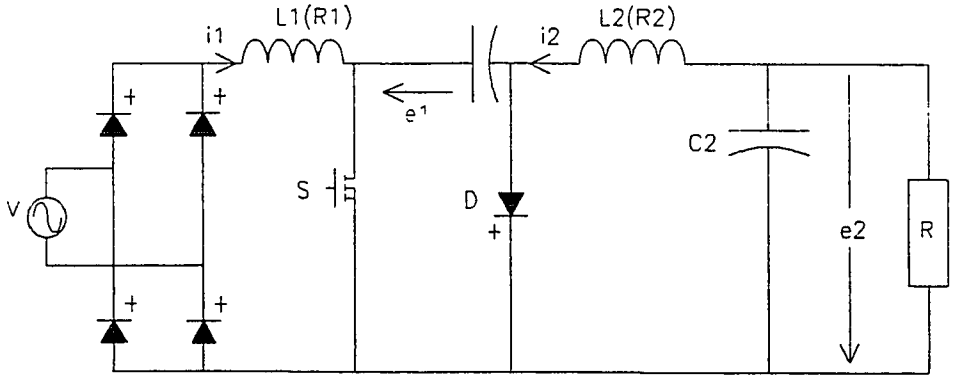

Figure 2-3: Single phase sinusoidal rectifier (Cuk derived) with step-up/step-down characteristics (ref. 3).

2.4 A Compact AC/AC Voltage Regulator Based on the AC/AC High-Frequency Flyback Converter

Barbi, Fagundus, and Kassaick (ref. 4) present another approach to the electronic transformer. The DC/DC flyback converter is transformed into an AC/AC unit by using bi-directional switches. In this respect, it is very close to the work originally done by Bowers, Garret, Nienhaus, and Brooks (ref. 1). Transfer function equations were obtained using state space manipulations. For values of duty cycle (D) less than 0.5, and with the appropriate selection of the inductor and capacitor values, the simplified DC relationship

of input and output voltage can be obtained. However, the following inequalities must hold true:

$$(1-D)^2 >> W^2 * L * C_o \tag{2-1}$$

$$(1-D)^2 >> \left(\frac{W*L}{R_o}\right) \tag{2-2}$$

$$\text{then } \left|\frac{V_o}{V_i}\right| = \frac{D}{1-D} \tag{2-3}$$

An input filter is designed for input current third harmonic distortion (THD) less than 3%. This would reduce the dominant harmonic to 3%, which leads to the following inequality:

$$W_s^2 * L_i * C_i \cong 32 \tag{2-4}$$

The circuit was built with the following components:

Input filter: $L_i = 280\text{mH}, C_i = 20\text{mF}$
Flyback Converter: $C_o = 80\text{mF}, L_m = 420\text{mH}$
$V_i = 50\text{V}, f_s = 12\ \text{KHz}$
$R_o = 13\Omega, T_{blank} = 1\text{ms}, T_{s1} = T_{s2} = 40\text{ms}$

Simulation and experimental results show some differences that are mostly attributed to the clamping circuitry used in the switches. After close examination of the work presented, it is evident that:

- The design and simulation for $D > 0.5$ was not performed. The simplified expressions of the transfer functions are not valid and the more complicated expression must be used.

- Neither compensation nor control techniques were suggested to stabilize the converter for different cases of input and load regulation requirements. This is important since the flyback (Buck-Boost) converter is inherently unstable because of the presence of a right-half plane zero in the converter's output to control transfer function.
- No load or line regulation data was given. Subsequently, it was unknown if the system was stable for any abrupt changes in load or line.

Finally, Barbi, Fagundus, and Kassaick discussed all aspects of the design including input filter, power factor calculation, and output current ripple, which are important factors for the practical implementation of the solid state transformer.

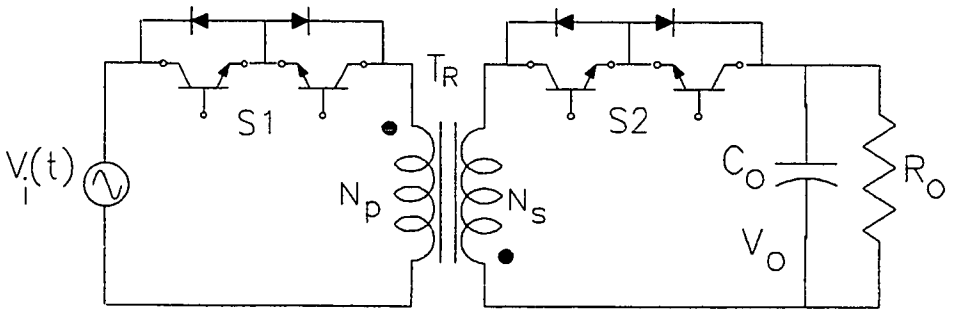

Figure 2-4: AC/AC voltage regulator based on AC/AC high-frequency flyback converter (ref. 4). The regulator uses bi-directional switches to handle AC voltage.

2.5 Resonant Mode Topologies

Significant work is in progress in resonant mode topologies, quasi-resonant converters, and soft-switching techniques (refs. 5-8). Most of these topologies are better suited for DC/DC conversion and are not presently applicable to the AC/AC case because

some of the designs have a large number (typically 12) of switches (refs. 7-9). If these designs are used in the AC/AC system, bi-directional switches must be used; this doubles the number of switches needed. Also, these topologies convert energy in two stages (AC⇒DC⇒AC), so there is a possibility of energy loss (in the total conversion) and reduced efficiency.

3. ANALYSIS METHODS FOR SWITCH MODE REGULATORS

3.1 Analysis Methods as an Important Tool in the Design of Converters

To fully understand and design a power conversion system, the proper design and analysis tools are necessary. These design and analysis tools must describe and model the behavior of the converter under different states and modes of operation. They must also reflect operating conditions such as extreme load and line disturbances. The tools should provide stability information and the criteria for design and be able to evaluate the performance of the final design according to established specifications and guidelines.

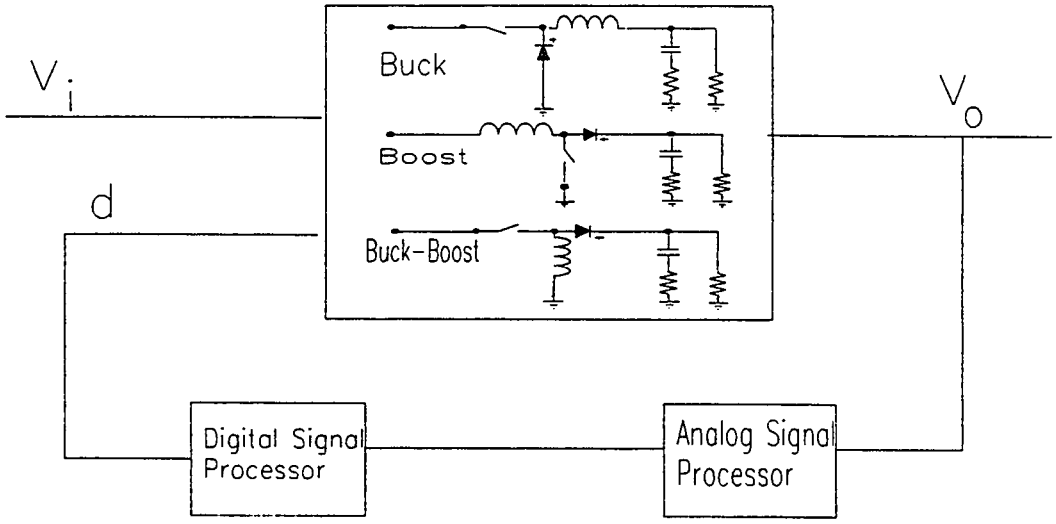

Figure 3-1: Standardized control module for switching converters (ref. 11). The figure shows the general form of a converter with V_o being fed to the analog signal processor containing the attenuator, comparator, and compensation. This feeds the digital signal processor, which generates the PWM signal that drives the converter switches by varying the duty cycle D.

In general, the switching converter (Figure 3-1) contains three basic functional blocks. They can be identified as the power stage, the analog signal processor (comparator and compensation network), and the digital signal processor (PWM duty cycle generator).

and compensation network), and the digital signal processor (PWM duty cycle generator). The switching regulator has two main nonlinearities. The first, residing in the power stage, is due to both the ON-OFF operation of the power switch and different circuit topologies attendant to the respective time intervals. The second exists in the digital signal processing system and accomplishes the analog-to-discrete-time duty cycle conversion.

3.2 Need for Analysis Methods

Topology manipulation and state-space averaging techniques were used to obtain linearized models for various power stages in both frequency domain and discrete time analysis (refs. 10-12). The analysis and behavior of the digital signal generator was developed (ref. 13) and provided the analysis of magnitude and phase of the transfer function of the pulse width modulator.

Once the combined frequency response of the power stage and the digital signal processor is obtained, the complementary analog signal processor frequency response can be designed to provide the desired converter control performance. Because of the presence of the power stage second-order output filter, very poor phase margin invariably exists if proper compensation is not provided in the analog signal processor. Conventional frequency response shaping techniques can be used, but they become grossly ineffective because of variations of power/control component parameters resulting from tolerances, environment, and aging. More importantly, external reactive loading (e.g., capacitor banks), which often are not fully defined during the regulator development, may render ineffective the compensator originally conceived for an assumed resistive load.

All of the above make it mandatory for the designer to seek analysis tools that will provide insight into the behavior and operation of the converter under different conditions throughout the life of the regulator. Also, these tools will enable the accuracy and precision demanded by the specifications to be predicted.

3.3 State-Space Averaging Technique

The state-space averaging technique (ref. 10) is the most widely used and accepted analysis method among power electronics specialists. It starts with the exact state-space description. Based on a practical assumption that the regulator output ripple is small, the model averages the exact state-space descriptions (of the respective power stages) corresponding to distinct time intervals over a single period of operation. The culmination of the averaging process is an equivalent linear circuit power stage representation about a quiescent operating point. The power stage model is then combined with the linear analog signal processor to perform the small signal analysis for a complete regulator.

A complete derivation using the state-space averaging method is provided and is applied to the Buck-Boost regulator to derive the output to input transfer functions as well as the output to the duty cycle transfer function (App. A). Here the method is used to derive the transfer function for the three basic converter topologies (Buck, Boost, and Buck-Boost) with resistive, capacitive, and inductive loads (results only).

The Canonical form (ref. 10) has a fixed topology and contains all the essential input-output and control properties of any switching converter regardless of its detailed configuration. By using this form, different converters can be characterized to tables

stored in a computer data bank to provide a useful tool for computer aided design and optimization. The Canonical form culminates the work done by Middlebrook and Cuk. It represents the results obtained by state-space averaging techniques in a concise, tabulated form.

3.4 Standardized Control Module for DC/DC Switching Regulators

Lee, Yu, and Mahmoud (ref. 11) studied the three basic switching regulators (Buck, Boost, and Buck-Boost) employing a multiloop control model and characterized them by a common small-signal block diagram. Employing this unified block diagram representation, regulator performance such as stability, audiosusceptability, output impedance, and step load transient are analyzed. Key performance indexes are expressed in simple analytical forms. Most importantly, the performance characteristics of the three regulators are shown to exhibit common properties. This is because of a unique multiloop scheme that nullifies the positive zero (right-half plane zero is present in the output-to-control transfer function because of parasitics). This scheme provides adaptive compensation to the moving poles of the Boost and the Buck-Boost converters. In turn, this allows a simple unified design procedure to be devised for selecting the key control parameters for an arbitrary given power stage configuration and parameter values. That is, all regulator performance specifications can be met and optimized concurrently in a single design attempt avoiding trial and error iterative attempts commonly used by designers. Figure 3-2 details the block diagram of a unified small signal representation.

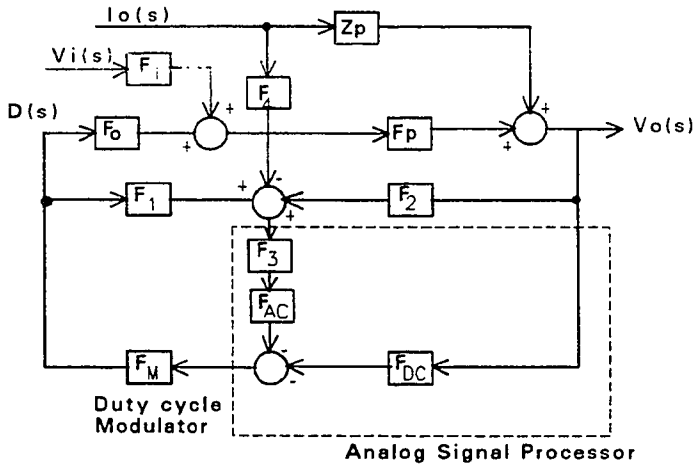

Figure 3-2: Unified small signal representation of the standardized control module of a switching converter (ref. 11).

The power stage transfer functions model incorporates all possible forms of small signal disturbances including the line disturbances $\hat{V}_i$, the load disturbances $\hat{I}_o$, and the duty cycle disturbances $\hat{d}$. It also provides both DC and AC error signals to the analog signal processor. In the unified small signal model the symbols are defined as follows:

$F_P(s)$: equivalent output filter transfer function.

$F_1(s)$: input voltage gain ($F_P * F_1$ represents the open loop input to output transfer function)

$F_D(s)$: duty cycle gain ($F_D * F_P$ represent the duty cycle to output voltage gain)

$Z_p(s)$: the output impedance of the open-loop converter power stage ($Z_p \times \hat{I}_o$ represents the open loop output voltage variation caused by load current disturbance)

$F_1(s)$ and $F_2(s)$ together provide the small-signal low-frequency AC inductor (or magnetic flux) current caused by the disturbances from the output voltage $\hat{V}_o$ and the duty cycle $\hat{d}$. It also should be noted that a

feed-forward path through F_1 exists for the Boost and the Buck-Boost converters. This is because the inductor is separated from the output filter capacitor by a switch. As a result, in the small signal model the equivalent inductance is modulated by the duty cycle of the switch.

$F_3(s)$: impedance function employed to convert the inductor current or magnetic flux into an AC loop error voltage $\hat{V}_{AC}$ across the sensing winding

$F_4(s)$: transfer function characterizing the amount of disturbance of the inductor current because of load disturbance

$F_{DC}(s)$: the transfer function of the combined DC loop and compensation loop

$F_{AC}(s)$: the transfer function of the AC loop

$F_m(s)$: the transfer function of the duty cycle pulse modulator

3.5 Simplified Analysis of PWM Converters Using a Model of a PWM Switch

The third analysis method is the simplified analysis of PWM converters using the model of the PWM switch by Vorperian (ref. 12). In this method, a new, simple, circuit-oriented analysis method for PWM converters, which uses the model of the PWM switch, is developed. The PWM switch model is used in the same way the model of the transistor is used in the analysis of electronic amplifier circuits. The PWM switch is presented as a three-terminal nonlinear device which represents the total nonlinearity in a PWM converter just as the transistor represents the total nonlinearity in an electronic amplifier. Hence, as one does not linearize the entire equations of an amplifier along with the Ebers-Moll equations of the transistor to determine its DC and small-signal characteristics, one does

not need to linearize the entire equations of a PWM converter (as is done in the case of state-space averaging, circuit averaging, and hybrid modeling).

Using this PWM switch model, PWM converters can be easily analyzed for DC and small-signal characteristics with standard electronic circuit analysis programs in closed-loop operation without the need for special programs. This method relies on the identification of a three-terminal nonlinear device (the PWM switch), which consists of only the active and passive switches in a PWM converter. Once the invariant properties of the PWM switch are determined, an average equivalent circuit model for it can be designed. This model is versatile enough to easily account for storage-time modulation of bipolar-junction transistors (BJTs). The DC and small-signal characteristics of a large class of PWM converters can be obtained by the simple substitution of the PWM switch with its equivalent model shown in Figure 3-3.

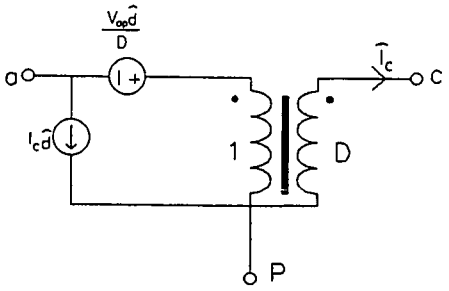

Figure 3-3: Simplified model of the three-terminal PWM switch operated in the continuous conduction mode (ref. 12).

The advantage of using the PWM switch model is that it allows many PWM converters to be analyzed using simple linear electronic circuit analysis programs (e.g., P-SPICE, MICRO-CAP). These programs allow for user-defined models (macros) without

recourse to special programs that manipulate state-space equations. The PWM switch model was used in developing a new current-mode control model (ref. 14), which disclosed a pair of complex right-half plane zeros in the current feedback loop, and three poles in the control-to-output transfer function. These features not revealed by the previous state-space averaging models, clearly explain the open-loop instability of current-mode control. The model is invariant for all converters and has no frequency dependent parameters. The model also has good results up to half the switching frequency.

3.6 Method of Choice

The state-space averaging technique was the method of choice for the analysis of the solid state transformer. Since the models were already successfully developed and used on DC/DC converters, they were adapted to be used on the AC/AC case. The 60 Hz input signal can be considered quasi-steady-state with respect to the 50 kHz switching signal. The two latter methods were useful in understanding the different tools and methods being developed and used in industry and research labs. Some of these techniques and methods supplement and reinforce the simple state-space method to obtain more information about the closed-loop system. However, for first-order approximation and accuracy, the state-space average models are sufficient.

4. CONVERTER TOPOLOGIES AND CONTROL DESIGN

4.1 Modes of Operation

This chapter reviews the Buck-Boost converter (Figure 4-1) used as the basic building block in the solid state transformer design and its mode of operation and control methods. The converter may be operated in one of two modes: the discontinuous or continuous inductor current modes.

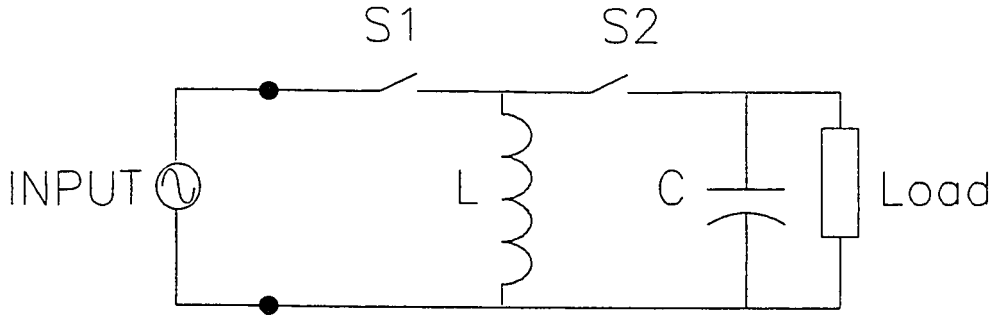

Figure 4-1: AC/AC Buck-Boost converter.

The choice of the operational mode has a great effect on the overall characteristics. The control method can help to minimize the problems associated with any topology and operational mode. Four control methods are examined: direct duty cycle control, voltage feed-forward, current mode (multiloop) control, and leading-edge modulation.
One common principle that applies to the converter regardless of operational mode is that in steady state operation the voltage across the inductor, averaged over each switching cycle, must equal zero.

4.2 Discontinuous Mode Operation

In the discontinuous current mode, the inductor current is zero (hence discontinuous) during the last part of each switching cycle. During the first part of the cycle, the inductor current increases from zero, storing energy from the input. During the second part, all of the stored energy is discharged into the load, pumping energy from input to output. By examining the discontinuous current waveforms shown in Figure 4-2, three distinct operational states can be identified.

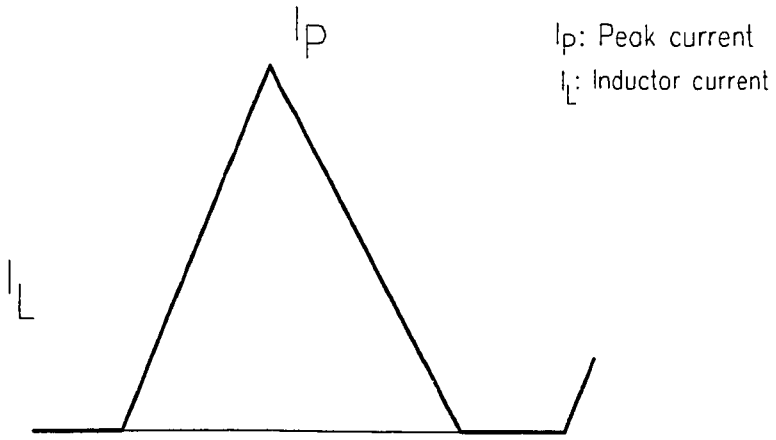

Figure 4-2: Discontinuous inductor current waveform. The current in the inductor goes to zero for a period of the switching cycle.

The three operational states are:

a. The transistor ON time, T_{ON}, where the inductor current rises from zero to the maximum value, i_{max}. This peak value is equal to the energy stored in the inductor, $LI^2/2$, at the end of T_{ON} period.

b. The transistor OFF time, T_{OFF}, where the inductor voltage reverses and its stored energy forces the same peak current to flow through the transistor S_2. During

transistor S_2 conduction time the inductor current drives the output and linearly decreases to zero

c. When the current reaches zero the inductor has no more energy. The current in all switching elements is zero for the remainder of the switching period.

4.2.1 Discontinuous mode boundary– When load current increases, the control circuit causes transistor T_{ON} or duty cycle to increase. Peak inductor current then becomes greater and switch conduction time, T_d, must also increase. Consequently, an increase in load current causes a steady state reduction in idle time, T_i. When load current increases to a certain level, T_i becomes zero and the discontinuous mode boundary is reached. If the load current is further increased, the inductor current will no longer discharge to zero every cycle and continuous mode operation results. The closed-loop circuit will become unstable because the loop gain compensation required for stable discontinuous mode operation is not adequate to prevent oscillation in the continuous mode. It is imperative for the control circuit to sense and limit the inductor current to prevent crossing the mode boundary.

In the discontinuous current mode it is easy to get excellent closed-loop response when correcting disturbances that result from large step changes in line voltage and load current. This is because the inductor always starts each switching cycle with zero stored energy. This makes it possible for the control circuit to obtain the energy level required (from zero to full output) on a cycle by cycle basis. The inductor "disappears" from the small signal closed-loop characteristics, leaving only the output capacitor with its

90-degree phase lag. The resulting single-pole characteristics are inherently stable and easy to deal with in closing the loop. The right-half plane zero, which severely limits closed-loop response in continuous mode, is not present as shown later in equation 4-4.

There are disadvantages to the discontinuous mode. First, there is high peak current through the transistors and the output capacitor. This requires semiconductors with higher current capability and places extreme burden on the output capacitor ESR and RMS current rating requirements. The second disadvantage is poor open-loop line and load regulation. The basic steady state equation for the Buck-Boost converter in discontinuous mode is (ref. 15):

$$V_o = V_{in} D \sqrt{\frac{R_o}{2Lf}} \tag{4-1}$$

It is evident from equation 4-1 that if the duty cycle is fixed, V_o varies directly with V_{in} and the square root of the load resistance, R_o. In other words, the open-loop line and load regulation are poor. Hence, the duty cycle must be changed considerably by the control circuit to maintain the desired output voltage under the full range of line and load conditions.

4.3 Control Methods for the Discontinuous Mode of Operation

There are three methods of control in the discontinuous current mode of operation. They are: direct duty cycle control, voltage feed-forward control, and current mode control.

4.3.1 Direct duty cycle control– The oldest and most commonly used method is implemented in most control IC's (e.g., Unitrode UC1524). The switch duty cycle is varied directly with the control voltage. The control voltage is the result of comparing the output voltage and a constant amplitude sinusoid representing the desired voltage. The disadvantages of this method are:

(1) No voltage feed-forward signal is provided to anticipate the effects of input voltage changes. The method suffers from poor open-loop line regulation and requires higher loop gain to achieve specifications.

(2) The output filter capacitor is part of the closed-loop system and introduces a phase lag that delays correction of V_{in} changes.

The basic equations of the discontinuous direct duty cycle control (ref. 15) are:

$$D = \frac{V_C}{V_S} \tag{4-2}$$

where D is the duty cycle of the switches, V_s represents the amplitude of the PWM sawtooth ramp, and V_c is the amplitude of the control voltage.

Output to input relationship:

$$\frac{V_o}{V_{in}} = D\left(\frac{R_o}{2Lf}\right)^{1/2} = \frac{V_c}{V_s}\left(\frac{R_o}{2Lf}\right)^{1/2} \tag{4-3}$$

Output to control relationship:

$$\frac{V_O}{V_C} = \frac{V_{in}}{V_s}\left(\frac{R_o}{2Lf}\right)^{1/2} H_e(s) \tag{4-4}$$

where R_o is the output resistance and R_C is the ESR of the output capacitor.

$$H_e(s) = \frac{1 + s/w_z}{1 + s/w_p},\ w_p = \frac{2}{R_o C},\ w_z = \frac{1}{R_C C} \tag{4-5}$$

4.3.2 Voltage feed-forward control– This control method functions exactly like direct duty cycle control with one key exception: the sawtooth ramp used for PWM is not constant amplitude, but varies in direct proportion to the input voltage and causes the duty cycle to vary inversely with input voltage, V_{in}, as well as directly with the control voltage, V_c. Open-loop line regulation is very good and much less gain is required to achieve good dynamic response.

The basic relationships of discontinuous voltage feed-forward control (ref. 15) are:

$$D = \frac{V_C}{V_S},\ V_S = \frac{V_{in}}{K},\ K = \frac{V_{in} D}{\max V_C} \tag{4-6}$$

$$\frac{V_o}{V_{in}} = D\left(\frac{R_o}{2Lf}\right)^{1/2} = KV_C\left(\frac{R_o}{2Lf}\right)^{1/2} \tag{4-7}$$

$$\frac{V_O}{V_C} = K\left(\frac{R_o}{2Lf}\right)^{1/2} H_e(s) \tag{4-8}$$

where $H_e(s)$ is the same as equation 4-5.

Inherent good line regulation is guaranteed because of the following relationship:

$$\frac{V_O}{V_{IN}} = 0 \tag{4-9}$$

4.3.3 Current mode control– The newest control method also controls the duty cycle by comparing the control voltage to a fixed frequency sawtooth ramp. An inner, second control loop compares the peak output transistor current to the control voltage, V_c. The results of this method are extremely significant. All of the problems of the direct duty cycle control methods are corrected. In addition to having a voltage feed-forward characteristic with instantaneous open-loop response to input changes, current mode control eliminates the inductor filter pole because this pole is inside the inner loop. This reduces the two pole second-order filter, which is not easy to compensate, to a single pole (the filter capacitor) and permits the design of simpler compensation networks.

The basic relationships for discontinuous current mode control (ref. 15) are:

$$\frac{V_o}{V_{in}} = D\left(\frac{R_o}{2Lf}\right)^{1/2} = KV_C\left(\frac{R_o}{2Lf}\right)^{1/2} \tag{4-10}$$

Control voltage V_C is given by:

$$V_C = \frac{V_O\sqrt{2}}{k\sqrt{LfR_O}} \tag{4-11}$$

Control to output gain is:

$$\frac{V_O}{V_C} = K\left(\frac{R_oLf}{2}\right)^{1/2} H_e(s) \tag{4-12}$$

where $H_e(s)$ is the same as equation 4-5.

Inherent good line regulation is guaranteed because of the following relationship:

$$\frac{V_o}{V_{in}} = 0 \tag{4-13}$$

4.4 Governing Equations for the Three Methods in the Discontinuous Case (ref. 16)

$$L_{max} = \frac{R_{min} * T * D_1^2}{2} \tag{4-14}$$

$$\text{where } R_{min} = \frac{V_o}{I_{omax}} \tag{4-15}$$

$$I_{max} = \frac{2 * P_{omax}}{D_H * V_{imin}} \tag{4-16}$$

$$\frac{\hat{V}_o}{\hat{V}_c} = \frac{V_o * D_1}{V_m * D} \sqrt{\frac{R * T}{2 * L}} * \frac{1}{1 + \frac{S * R * C}{2}} \tag{4-17}$$

$$D_1 = \sqrt{\frac{2 * L}{R * T}} \tag{4-18}$$

$$D_1 = \frac{V_{imin}(1 - D_2)}{V_o + V_{imin}} \tag{4-19}$$

4.5 General Remarks on Discontinuous Mode

Inspecting the output voltage to the control equation shows that the response is that of a first-order system. The gain is controllable by duty ratio adjustment. Device selection is constrained by $V_i + V_o$ and I_{max}. They are relatively higher than their continuous conduction counterparts. Because of the high inductor peak current, device

usage is inefficient in discontinuous conduction converters, limiting the circuit in this mode of operation to only low-power applications.

To determine the inductance (ref. 16) for a given requirement, a small dwell time duty ratio is assumed. The steady state off-time duty ratio, D_1, is then calculated. If D_2 is equal to zero, the converter will operate at critical current level at low line and at maximum load. This means that under startup conditions, the closed-loop converter could lapse into continuous conduction mode. This temporary behavior could be sufficient for the startup of a parasitic oscillation.

To avoid this problem related to transient conditions, the inductance value constitutes a less effective output filter. This requires the use of large capacitance values with stringent ESR requirements to meet a given output ripple specification. Another method to avoid this problem is to compensate the converter loop for both single-pole and two-pole responses because the discontinuous conduction converter has the response of a first-order system under steady state conditions. This is because in the discontinuous conduction mode, the inductor current, does not behave like a true state variable. As a result, the order of the state-space averaged model is reduced by one. The first-order system response property of the discontinuous conduction converter permits closing the feedback loop with simple or no compensation.

It is not uncommon to design the converter to operate in both conduction modes for reasons of efficiency or component size reduction. In this case, the converter is

allowed to operate in discontinuous conduction mode at light load and continuous conduction mode at heavier load

4.6 Features of the Discontinuous Conduction Mode

The features of the discontinuous conduction mode are: high peak inductor current; high noise level; inefficient use of switching devices; high output voltage and current ripple; and a smaller magnetic core for the inductor, compared with the continuous conduction mode converter.

4.7 Continuous Mode Operation

In continuous mode operation the inductor current never remains at zero during any part of the switching cycle. Compared to the discontinuous mode for the same application parameters, the continuous mode requires much greater inductance. The inductor ripple current is small compared to the full load output current. The inductor current is shown in Figure 4-3. Because the inductor current is never zero, there is no idle time in the continuous mode and only two operational states during each switching cycle.

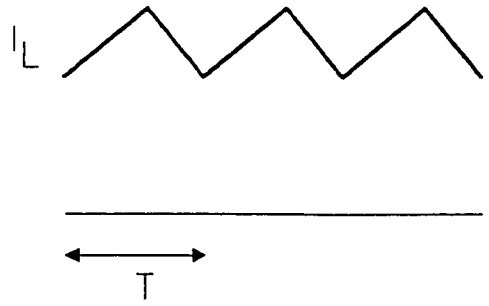

Figure 4-3: Continuous inductor current waveform. The current rides on a sinusoidal wave and never remains at zero for a period of the cycle. The current may reverse direction through the inductor.

The two operational states are:

a. During transistor ON time, T_{ON}, the inductor current, I_L, increases from an initial value greater than zero to a higher value, replacing the inductor energy given up during the OFF time. Current and power are drawn from the input.

b. When the transistor is off, the output transistor conducts for the rest of each cycle. I_L declines to the initial value, never reaching zero, but giving up energy to the output. The inductor current rides on a sinusoidal wave. It is possible that the current will go through zero at the zero crossing points of the sinusoidal wave, but the current still can be considered continuous. This is because the current does not remain at zero for a period of the cycle. The current may reverse direction through the inductor because of the intrinsic diode of the bi-directional switch. This is quite different from the DC case where the current never crosses zero.

4.7.1 Continuous mode boundary– When the load current decreases, the duty cycle and the inductor ripple current do not change, but the average inductor current declines proportionally, $I_o = (1 - D) I_L$. At a certain critical load current level, the inductor current reaches zero at the minimum of the ripple waveform. This is the boundary for continuous mode operation. If the load current further decreases, the third state idle time appears, and the current operates discontinuously. Steady state regulation degrades radically. In a continuous mode regulator, the load current must not be allowed to drop below the critical level where the boundary is crossed. The minimum load requirement is a disadvantage of continuous mode systems.

Small signal response of continuous mode regulators is much worse than discontinuous circuits because of the two pole characteristics of the resonant inductor-capacitor (LC) filter. It also has a right-half plane zero in their loop gain characteristic (Boost and Buck-Boost topologies only). Unlike the discontinuous mode, the output to input voltage relationship is as follows:

$$V_o = \frac{V_{IN} * D}{(1-D)} \tag{4-20}$$

This reveals that the output voltage is totally independent of output current or resistance, depending only upon V_{in} and D. The duty cycle does not change with steady state changes in load current, but D must be changed to make correction for changes in V_{in}.

4.8 Control Methods for the Continuous Mode of Operation

There are three methods of control in the continuous current mode of operation: direct duty cycle control, voltage feed-forward control, and current mode control.

4.8.1 Direct duty cycle control– In this control method moderately high-loop gain is required to correct the inherent poor open-loop line regulation.

The basic relationships of continuous direct duty cycle control (ref. 15) are:
Steady state equation:

$$\frac{V_O}{V_{in}} = \frac{D}{1-D} = \frac{V_{in}}{\left(\frac{V_S}{V_C} - 1\right)} \tag{4-21}$$

Control voltage:

$$V_C = V_S \frac{V_O}{V_{in} + V_O} \tag{4-22}$$

$$\frac{V_O}{V_C} = \frac{V_{in}}{V_S}\left(1 + \frac{V_O}{V_i}\right)^2 F1(s) H_e(s) \tag{4-23}$$

$$H_e(s) = \frac{1 + s/w_Z}{1 + (s/w_O)/Q + (s/w_O)^2} \tag{4-24}$$

$$F1(s) = 1 - \frac{sL}{R}\frac{V_o(V_o + V_i)}{V_i^2} \tag{4-25}$$

4.8.2 Voltage feed-forward control– This method is not recommended for the Buck-Boost converter.

4.8.3 Current mode control– The basic relationships of continuous current mode control (ref. 15) are:

$$I_O = I_L(1 - D) \tag{4-26}$$

$$I_L = KV_C \tag{4-27}$$

$$K = \frac{\max I_L}{\max V_C} \tag{4-28}$$

Steady state equation:

$$\frac{V_o}{V_{in}} = \frac{D}{1 - D} = KV_C R_O \frac{V_{in}}{V_O + V_{in}} \tag{4-29}$$

$$\frac{V_O}{V_C} = KR_O \frac{V_{in}}{(2V_O + V_{in})} f1(s)\, H_e(s) \tag{4-30}$$

$$H_e(s) = \frac{1 + s/w_Z}{1 + s/w_p} \tag{4-31}$$

$$F_1(s) = 1 - \frac{sL}{R}\frac{V_O(V_O + V_{in})}{V_{in}^2} \tag{4-32}$$

$$\frac{V_o}{V_{in}} = \frac{V_o^2}{2V_oV_{in} + V_{in}^2} H_e(s) \tag{4-33}$$

4.9 General Remarks on Continuous Mode

A close examination of the equation indicates that the system has a zero in the transfer function. By virtue of the negative sign within the expression, the zero is located in the right half of the complex frequency domain. Also, the corner frequency of the effective output filter represented by $H_e(S)$ is duty ratio dependent. This means the actual loop gain response at high and low duty ratios would exhibit two distinct resonant frequencies for the same filter elements. This is due to constant periodic changes between two different topologies during switching. The Buck-Boost converter is highly nonlinear. Beside having a duty ratio dependent output filter, the right-half plane zero is both duty ratio and frequency dependent.

4.10 Explanation of the Dynamics of the Right-Half Plane Zero

The bode plot of the right-half plane zero has the characteristics of a rising 20 db/decade gain with a 90 degree phase lag instead of the more usual lead. It is

therefore extremely difficult to compensate this effect by normal loop compensation techniques. If compensating for the rising gain is attempted, the phase crosses 180 degrees and the converter oscillates. If compensating for the phase is attempted, the overall gain increases with frequency and the gain crossover frequency becomes difficult to attain. The only alternative is to roll off or lower the gain crossover frequency far below its desired value (i.e. smaller bandwidth). This makes the continuous mode converter very difficult to compensate because it is sacrificing the dynamic response (transient response).

4.11 Conditions for the Right-Half Plane Zero to Occur

When the load current increases, the output capacitor voltage immediately starts to drop. The resulting error voltage temporarily increases the duty cycle, D, causing the inductor current to rise to accommodate the increased load. However, it may take many cycles for the inductor current to complete the rise. During this time, increased D makes (1 - D) smaller, so the output current is temporarily decreased. This decrease is the opposite of what is desired. The additional lag of the right-half plane zero inevitably forces the loop gain crossover frequency to be much lower than otherwise required.

4.12 Controller Design for the Solid State Transformer

After careful investigation of modes of operation for the Buck-Boost converter and different control methods that can be used, an educated choice of which is best for the type of application can be made. In this case, the choice can be made with the knowledge that (a) the Buck-Boost converter in the bi-directional switch configuration does not lapse

into discontinuous mode unless the current is forced to go to zero, and (b) the high current in the circuit can be as high as four times the full load current (ref. 16). The decision was made to remain in the continuous mode and to control with direct duty cycle. Current mode control could be used in future designs.

In this section, the controller for both cases will be presented. Bode plot, phase margin, and gain margin for the direct duty cycle control method will be examined. A full set of diagrams is presented in Appendix E.

For either case of control, the power circuit parameters have to be designed. Some parameters are:

- Input voltage range
- Output voltage range (this determines the range of duty cycle needed for the converter)
- Output current range
- Allowable ripple (this determines the range of ESR of the output capacitance)
- Load impedance—resistive, inductive, or capacitive (this dictates the governing equations)

The most critical parameter is the output load impedance because it can dictate the position of poles and zeros. A good knowledge of the load being driven is very important because this could adversely affect the stability and performance of the complete system and render the compensation circuit useless if not properly taken into consideration. Also of special importance is the ESR of the output capacitor because it contributes a zero in

the left-half plane. The ideal performance characteristics happen if the gain has a -20 db/decade roll off and a phase of -90 degrees or as close as possible to a one-pole system. This provides the optimum phase and gain margins as well as bandwidth.

Once the compensator is designed and the desirable load range is taken into account (resistive, inductive, capacitive, or a combination), the converter becomes rather insensitive or "load independent" to load changes. This is because the compensator will actively nullify the effects of load change. The converter must be tested at these loads and the operation verified.

4.13 Continuous Mode Direct Duty Cycle Control

The converter has a double pole at $w_o = \frac{1-D}{\sqrt{LC}}$ because of the filter circuit. It has a zero because of the ESR of the output capacitor at $w_z = \frac{1}{R_C C}$ where R_C is the ESR value. It also has a zero in the right-half plane at $W_{RHP} = \frac{L}{R} * \frac{V_o(V_o + V_i)}{V_i^2}$. The right-half plane zero causes rising gain at +20 db/decade and decreasing phase at -45 degrees/decade, which is hard to compensate. The two poles contribute -180 degrees of phase at one decade above W_o. The ESR zero contributes +90 degrees at one decade above W_Z. The location of the ESR zero can have two extremes according to the value of the ESR found by measurement or from manufacturer data sheets. The location of the right-half plane zero can have two extremes at the extremes of operation. Three combinations can occur:

- $W_{Z1(ESR)}$ is less than $W_{Z1(RHP)}$

- $W_{Z1(ESR)}$ is less than $W_{Z2(RHP)}$
- $W_{Z2(ESR)}$ is greater than $W_{Z2(RHP)}$

The bode plot is different for each case and the compensator has to take into account all cases.

The placement of a compensator with three poles and two zeros stabilizes the system. The first pole will be at low frequency to meet regulation requirements. The two second-order filter poles will be compensated by two zeros at W_o. Two additional poles cancel the ESR zero and the right-half plane zero. The location of the two poles can be adjusted by trial and error or by the K-factor method (ref. 17). Above the crossover frequency these two poles are necessary, otherwise the gain would stay flat, or even rise, causing instability at higher frequencies. Since the location of the right-half plane zero moves with resistance of the output and input levels, the two extremes should be considered. Also, the ESR zero is dependent on the ESR value, which varies with temperature, and the two extremes should be considered. The bode plots of a system before and after compensation are shown in Appendix E.

4.14 Continuous Mode Current Mode Control

The converter has a single pole at $W_P = \frac{1+D}{RC}$ and a single zero at $W_Z = \frac{1}{R_C C}$

where R_C is the value of ESR. It still has a right-half plane zero at

$W_{RHP} = \frac{L}{R} * \frac{V_o(V_o + V_i)}{V_i^2}$. The bode plot of this system shows that the phase margin is very

acceptable without compensation. But due to the dynamics of the system and the rising gain after the crossover frequency, compensation must be provided. This will avoid instability at higher frequencies where the gain emerges above 0 db. This could cause instability if the phase of the system was less than -180 degrees. This shift most commonly happens because of circuit parameter changes, temperature, or aging at higher frequencies. The location of the ESR zero can have two extremes according to the value of the ESR. The location of the right-half plane zero can have two extremes at the extremes of operation. Three combinations can occur:

- $W_{Z1(ESR)}$ is less than $W_{Z1(RHP)}$
- $W_{Z1(ESR)}$ is less than $W_{Z2(RHP)}$
- $W_{Z2(ESR)}$ is greater than $W_{Z2(RHP)}$

The bode plot is different for each case and the compensator has to take into account all cases. The compensator needed would have two poles to cancel the ESR zero and the right-half plane zero. The location can be determined by trial and error or the K-factor method. The trial and error method is not very exhausting since there are programs available that compute the phase margin and gain margin. They do not need any intervention from the user to do these tedious calculations. A program in Matlab using the control toolbox could set up a loop to calculate the phase margin, gain margin, DC gain, and the gain and phase crossover frequencies. This program would also determine the bandwidth of the system. A listing of this program is given for the direct duty cycle control method in Appendix E.

4.15 Leading-Edge Modulation Control

The fourth method that promises to solve the control problem is leading-edge modulation (ref. 18). Using the discrete average model mathematical derivation, it was suggested that to remove the right-half plane the following conditions must hold true:

- $R_C C > \frac{L}{D R_L}$
- Leading-edge modulation must be used. In leading edge modulation the PWM signal is turned OFF at the clock signal and is turned ON when the error signal intersects the ramp waveform.
- The feedback compensation must not average the ESR-generated output voltage switching ripple.

Digital modulation must be employed in this method to measure the loop gain accurately. It shows that loop gain crossover is much higher than can be ordinarily expected with a conventional trailing-edge-modulated Buck-Boost regulator. There are several disadvantages to this technique. Measurement of the control to output transfer function cannot be easily performed. Also, the positive zero elimination is dependent on the capacitor ESR value. This technique is susceptible to noise because the output voltage switching ripple is not filtered in the compensation network.

For this type of control method the control loop design uses a compensator that has two poles and two zeros. The first pole is placed at the origin for DC regulation. The two zeros are placed to obtain the maximum mid-band gain and a good phase margin in

the loop gain while minimizing the system transient response settling time. The first zero is placed just after the resonant frequency to avoid a conditionally stable system. The second zero is placed at approximately twice the frequency of the first zero. The second pole is placed to cancel the zero in the power stage that has been moved to the left-half plane.

5. HARDWARE IMPLEMENTATION AND EXPERIMENTAL RESULTS

5.1 Solid State Transformer Building Blocks

The solid state transformer shown in Figure 5-1 has the following basic building blocks:

- Buck-Boost converter containing the power inductor, the output filter capacitor, and a pair of bi-directional IGBT switches
- Driver circuits to drive the gates of the high-power IGBTs
- PWM generating circuit
- Feedback control structure that includes an error amplifier and frequency compensation circuit

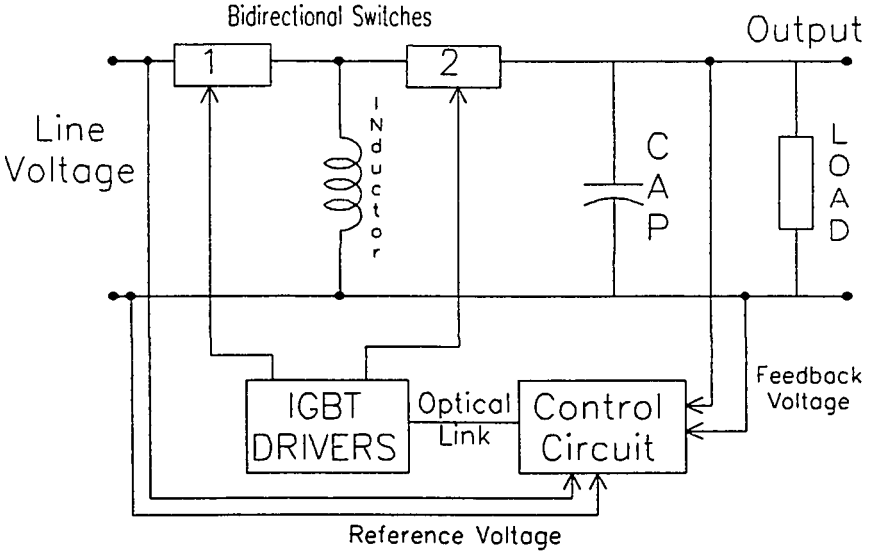

Figure 5-1: Block diagram of the solid state transformer. The complete system in its closed-loop form consists of the Buck-Boost converter, the IGBT PWM drivers, and the control circuitry.

5.2 Buck-Boost

The Buck-Boost converter is operated in the continuous mode direct duty cycle control as detailed in Chapter 4. In this method, the output voltage is attenuated and compared to an input reference voltage. The resulting error signal is used as an input to the PWM duty cycle generator that is fed to the driver circuits and drives the IGBT switches.

5.3 Bi-Directional Switch Design

The IGBT switches allow current to flow in both directions. This is achieved by bi-directional switch design as shown in Figure 5-2.

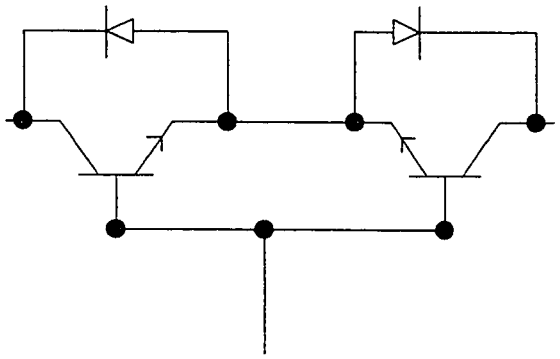

Figure 5-2: Bi-directional switch configuration consists of two IGBT switches connected back-to-back with the emitters and bases connected.

Two transistors are placed back-to-back with the emitters and bases connected. Bi-directional current flow is accomplished by installing flyback diodes across the emitter and collector of each transistor that, in this case, are intrinsic to the IGBTs. When both transistors are turned on, both are conducting. Depending on the current flow, the

transistor that is reverse biased is bypassed by its associated flyback diode. When both transistors are turned off, current is blocked in both directions. To turn the transistor switches on, the common base node must be forward biased with respect to the common emitter node. The biasing of these switches will be discussed later in the Section 5.5. The completed circuit with the switches is shown in Figure 5-3.

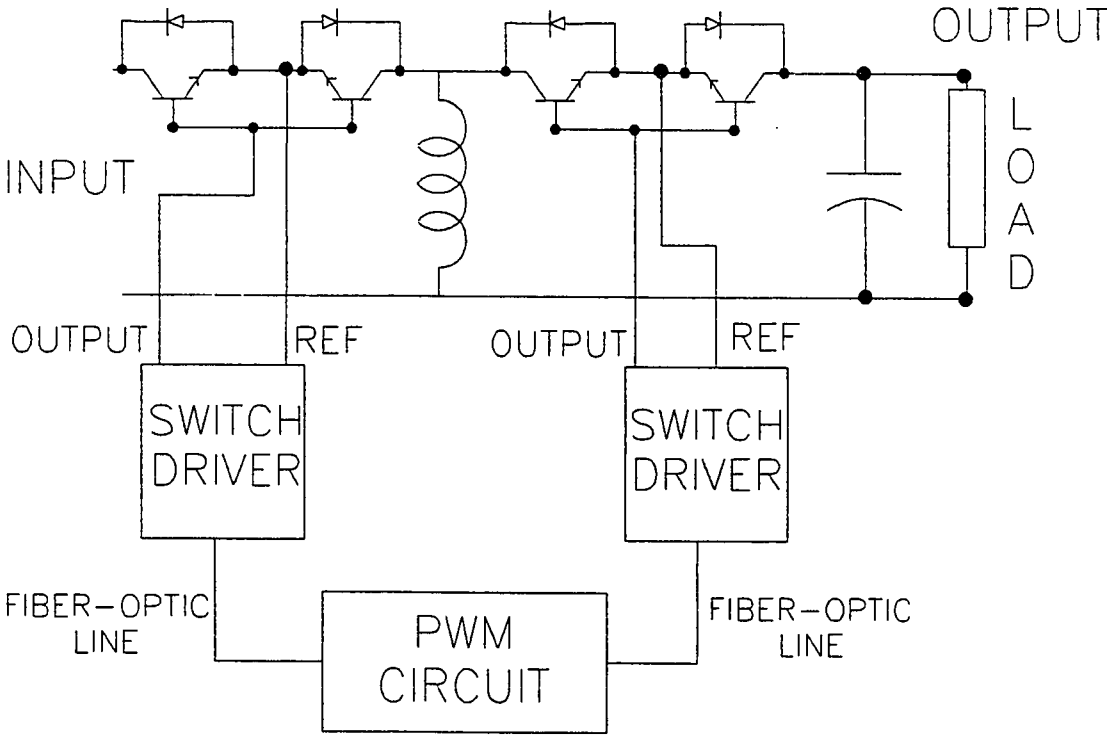

Figure 5-3: Solid state transformer block diagram with bi-directional switches. This is the same as Figure 5-1, but with the bi-directional switches in place and driver reference points indicated.

Power IGBTs were used to implement the switch design. The reasons for this selection were:

- Power IGBTs come equipped with flyback diodes incorporated.
- Bipolar characteristics of these switches ensure fast switching requirements.

- There is a low-power control circuit because of metal-oxide-semiconductor (MOS) gate characteristics.

Appendix C provides a parts list and specific data concerning the actual devices used.

5.4 Inductor Design

The main design consideration of the inductor depends on whether continuous or discontinuous current modes are chosen. Because the initial regulator design is to operate in continuous mode, the continuous mode values for the inductor as detailed in Chapter 4 will be used. Once the inductance value is determined, the selection of the core material and type can be made.

Core losses are directly proportional to switching frequency so a core material with very high permeability (μ = 1000-3000) is required. Because the inductor is designed to store energy, and high-permeability magnetic materials cannot store much energy, therefore a low-permeability gap, such as air, must be included in the design. Materials such as Moly-Permalloy store energy in the nonmagnetic binder used to hold the magnetic particles together so an air gap is not required. Solid toroids made from this material are sometimes used in switch mode designs. Ferrite is the most widely used material for switch-mode filter inductor applications. For that reason, a large variety of core sizes and types are available off the shelf. The double E core is a good choice because there is a broad range of sizes available. The air gap in the double E can also be adjusted to fine tune the design to limit flux density and inductance.

Knowing the material, type, inductance value, and peak current, a core can be selected from the manufacturers specifications. Once a specific core is selected, an inductor can be wound using recommended air gaps and inductance index charts. The core used in this project is a double E ferrite-type wound to approximately 0.10 mF. See Appendix B for the design details and core specification.

5.5 Driver Circuit Design

With a switching frequency of 50 KHz, it was necessary to switch the high-power IGBTs as fast as possible to achieve maximum performance. The longer the switching time of these semiconductor devices, the greater the heat stresses encountered during operation. Since the IGBTs are MOS devices, there is considerable oxide capacitance associated with the gate-to-emitter junction. Although steady state gate currents are quite low, current transients during turn-on and turn-off can be quite high depending on the selection of series gate resistors.

There are many MOSFET driver ICs available off the shelf designed to drive power MOSFETs. Unfortunately the performance required to drive two IGBTs used in this project is not available in a single package IC. A solution to this problem is to supplement a MOSFET driver IC with an additional stage consisting of a complementary pair of bipolar power transistors in an emitter follower arrangement (Figure 5-4). Because the IGBTs have to be forward biased with respect to their emitters, the driver circuits have to be referenced to that potential also (Figure 5-3). Therefore, each driver circuit must

contain its own positive and negative power supply that floats on the AC line being regulated.

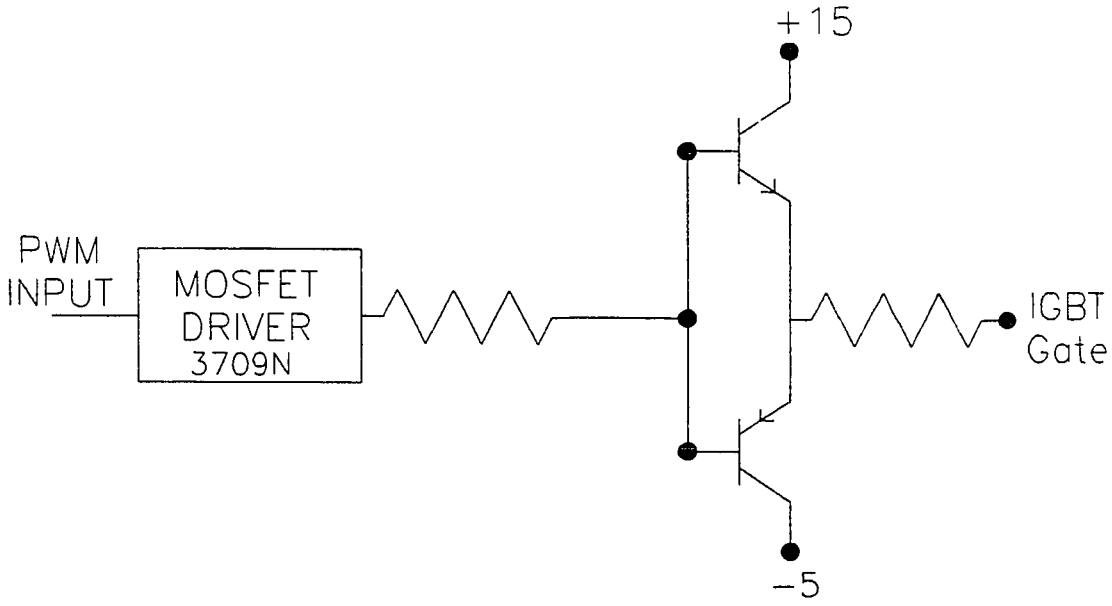

Figure 5-4: Emitter follower IGBT gate driver design.

In addition to the power supply requirements of the driver circuits, a means of receiving the PWM signal must also be considered. The solution to this problem is through optical isolation by means of optical transmitters, receivers, and fiber optic cables. An optical receiver is installed in both driver circuits to receive the PWM signal generated on a different board referenced to ground as shown in Figure 5-5. See Appendix B for the actual circuit diagrams and Appendix C for component data.

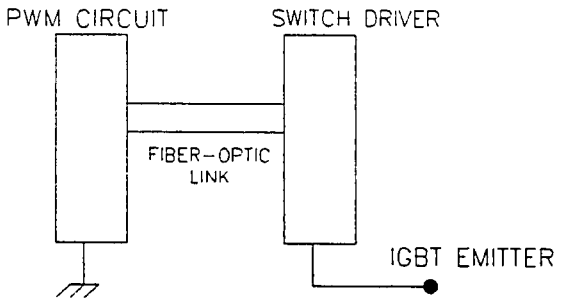

Figure 5-5: Optical isolation of driver circuits. Shown is the fiber optic link connecting the PWM generating circuit and the IGBT drivers that float over the IGBT emitter.

5.6 Feedback Path

The feedback path contains: (1) The error amplifier, which compares the output signal with the reference input. In order to achieve different duty cycles, either the potentiometer varies the output signal to attenuate the signal or varies the reference input signal. This also helps to minimize the open-loop gain variations between the two extremes of operation. (2) The compensation circuit, which is (in its general case) a three-pole two-zero compensator. (3) The phase detection and correction circuit, which senses the input and output and makes sure that the feedback is negative at all times. This is detailed in Figure 5-6. The specific circuit has not been implemented.

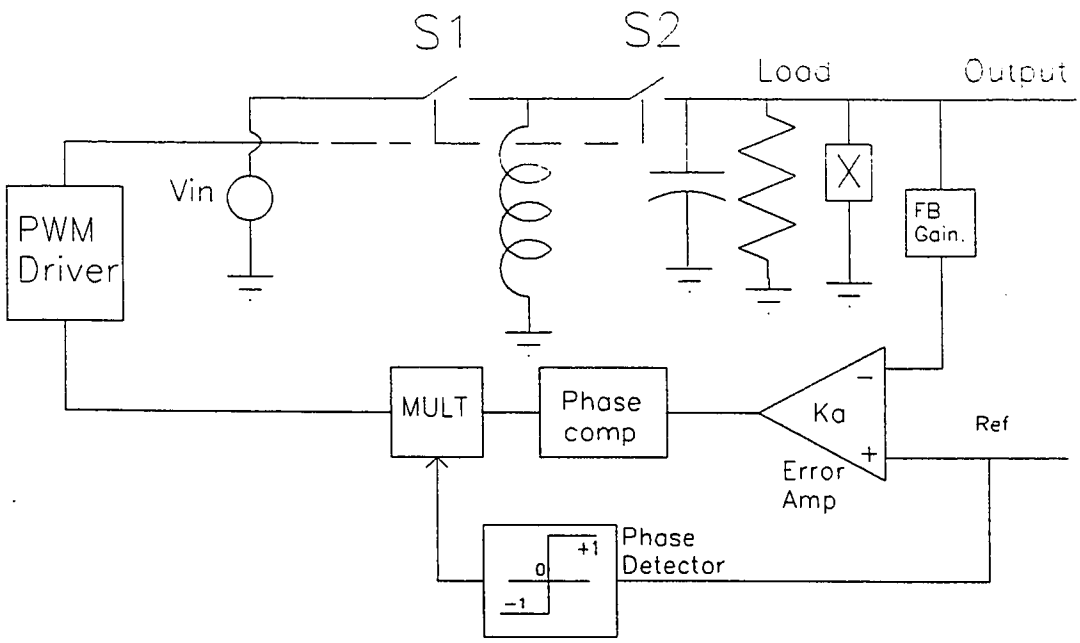

Figure 5-6: Solid state transformer closed-loop system block diagram. The figure shows details of the complete circuit including the Buck-Boost converter, the feedback gain, the comparator, the phase detector and compensator, and the PWM IGBT driver.

5.7 Transformer Design Specifications

1. Power is 1 kW

2. Input voltage maximum is 120v RMS

3. Duty ratio is controllable in the range of 0.25 to 0.75

4. Operation mode in continuous mode duty cycle control for initial design. A more robust leading-edge modulation or current mode control can be implemented in future designs.

5. Output voltage maximum is $V_{inmax} * \frac{D}{1-D}$ which has a maximum value of 360 V RMS.

6. Switching Frequency is 50 kHz naturally sampled so it does not introduce any lag to the converter. An initial design is done using a 555 timer chip. A more sophisticated PWM dedicated chip was designed and can be implemented in hardware for future designs.

The cutoff frequency is $f_c = \frac{1}{2\pi\sqrt{LC}}$. With the proper choice of inductor and capacitor values the corner frequency, f_c, can be chosen. Inductor, L, is equal to 85μH and capacitor, C, is equal to 25μF. These values yield the corner frequency that provides a high degree of attenuation to the 50 kHz frequency without providing significant attenuation or phase shift to the 60 Hz input frequency. F_o is a value that critically affects the compensator design, so where f_o is the resonant frequency of the output filter, $f_o = \frac{1-D}{2\pi\sqrt{LC}}$.

Current has to be limited at one of the two extremes of operation: maximum power and maximum current. For maximum power of 1 kW, P = 1000 watts = $\frac{V^2}{R}$ = $\frac{(360)^2}{R}$, therefore R = 129.6 Ω. For the maximum current, which was chosen to be 10 Amperes, P = 1000 watts = $I^2 * R = 100 * R$, therefore R = 10 Ω. So output resistance, R, is always in the range of 10 Ω to 129.6 Ω.

5.8 Compensator Design

By examining the output voltage to the duty cycle change transfer function:

$$\frac{\Delta V_o}{\Delta D} = \frac{V_{in}}{(1-D)^2} \frac{(1+s/w_z)(1-\frac{sDL}{(1-D)^2 R})}{1+\frac{sL}{R(1-D)}+\frac{sLC}{(1-D)^2}} \tag{5-1}$$

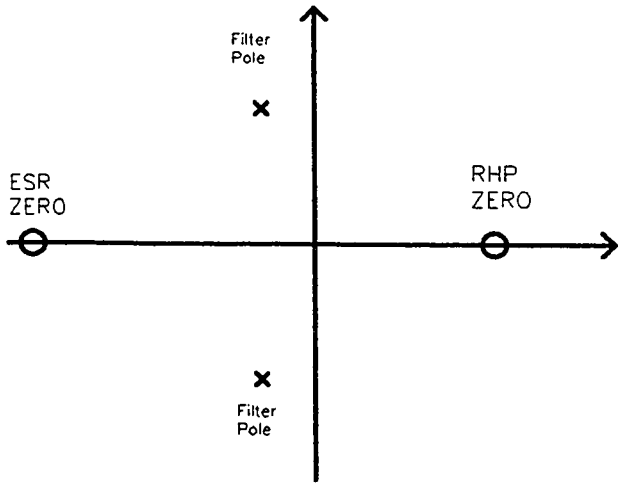

Figure 5-7: Pole- zero map for the solid state transformer. The plot shows the presence of the right-half plane zero, the left-half plane zero (because of ESR), and the conjugate filter poles.

Conjugate filter poles occur at $s = \frac{-1}{2RC(1-D)} \pm \frac{1}{2(1-D)RLC}\sqrt{L^2-4R^2}$, right-half plane zero occurs at $s = \frac{(1-D)^2 R}{DL}$, ESR zero occurs at $s = -\frac{1}{R_C C}$.

The system has two zeros and two poles. The two poles are caused by the output filter and are located at f_o and the two zeros are caused by the ESR and the right-half plane zero, which is inherent in Buck-Boost circuits operating in the direct duty cycle

continuous mode of operation. The ESR zero is located at $w_z = \frac{1}{2\pi * R_c C}$, and the right-half plane zero is located at $w_{RHP} = \frac{(1-D)^2 * R}{D * L}$.

For the compensator to be designed, a pole was placed at origin or at f< 1 Hz to provide enough gain at low frequencies to meet regulation requirements. The two second-order poles at f_o are compensated by two zeros at $f_z = f_o$. Two additional poles cancel the ESR zero and the right-half plane zero. The location can be adjusted by trial and error or the K-factor method and final simulation in Matlab to ensure stability and decent phase and gain margins. Although above the crossover frequency, these poles are necessary otherwise the gain will stay flat or, in the worst case, rise and cause instability at higher frequencies. The pole zero location for the compensator is shown in Figure 5-8.

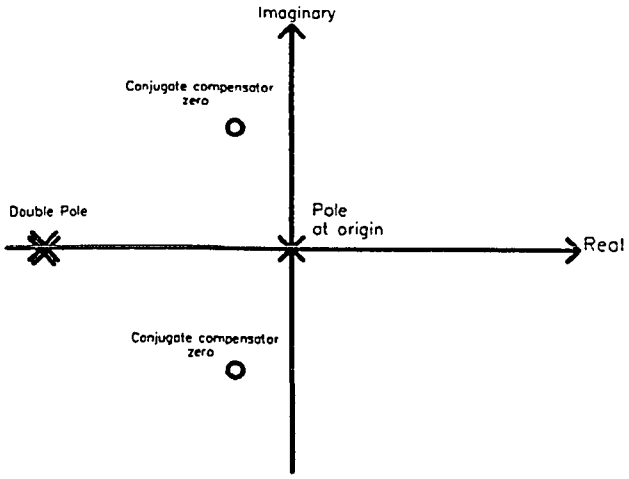

Figure 5-8: Pole-zero map for the compensator. The plot shows the location of the poles and zeros for the three-pole two-zero compensator.

The general expression for the compensator is:

$$G(S) = \frac{S*(1+S/W_z)^2}{(1+S/W_p)^2} \qquad (5\text{-}2)$$

The two zeros can coincide or can be different according to the desired phase margin.

5.9 PWM Circuit Design

A simple PWM circuit was designed based on the 555 timer IC and a simple resistor-capacitor (RC) circuit as detailed in figure 5-9. In addition to the 555 timer, a tri-state line driver IC was used to generate a complemented PWM signal required for the operation of the second switch of the transformer (S2). The output of the tri-state line driver are connected to the optical transmitters to supply switching information to the IGBT driver circuits as shown in Figure 5-3.

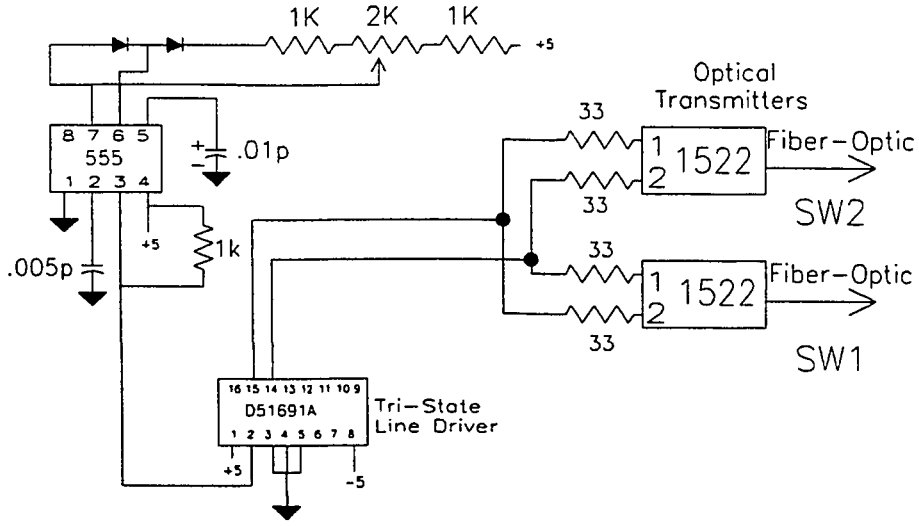

Figure 5-9: Complete PWM circuit design using a 555 chip.

A more advanced PWM technique using a dedicated IC was designed. This is a stepping stone for future hardware implementation. The Unitrode 3524A control chip is used in the voltage mode for regulating the output voltage. The built-in error amplifier senses the difference between the input and the output voltage and delivers a 0-5V signal to the internal PWM comparator and sets the duty cycle of the switches. It is supplied by a +15V supply. Local 0.1 uF bypass caps are used for the Vdd input (pin 15) and the Vref output (pin 16). See Figure 5-10 for the block diagram of the PWM circuit (ref. 19).

The onboard chip oscillator is programmed by the selection of a resistor and a capacitor. Because a single-ended output was used, minimum dead time was chosen and a 1000 pF capacitor was selected for C_t input (pin 7) as dictated by manufacturer data sheets. For 50 kHz operation R_t (pin 6) was selected to be 23 KΩ.

For test purposes, the PWM comparator and output logic can be disabled by holding the shutdown pin 10 high (+5V) using a jumper. This is useful for running the switched drivers directly from a variable square wave generator. The test generator is coupled through the open collector high-frequency NPN transistor to the open collector output of the "A" transistor (pin 12). The 0.0047 uF capacitor across the 100 KΩ resistor forces the test input transistor to quickly turn off.

The single-ended output of the "A" transistor is converted to a bi-polar output using a push-pull transistor circuit. When the output transistor is ON, base currents supplied to the upper NPN transistor and the output reaches approximately +15 V. The lower transistor is OFF because its PNP base drive is OFF with zero base emitter voltage.

When the output transistor is OFF, the upper transistor turns OFF because both its base and emitter are at +15V. The lower transistor turns ON, because its PNP base driver is ON and its emitter is at +15V. The output goes down to approximately -15V. The resistor in the supply leads limit the current during switching. This circuit inverts the output of the Unitrode 3524A. The circuit diagram is shown in Figure 5-10 (ref. 19). The block diagram and pinout of the Unitrode 3524A is shown in Figure 5-11 (ref. 19).

5.10 Experimental Results

The transformer was tested open-loop (without the feedback and compensation circuit connected). The loads used were that of a 1 kW fan and heater. The duty cycle was varied from minimum to maximum (D = 0.25 to 0.75). The input and output power were monitored for the AC case using the BMI 3060 Power Profiler meter (BMI, 335 Lakeside Drive, Foster City, California), which records both input and output voltage, current RMS values, and true power. From these values efficiency can be calculated. The DC case was monitored using the lab rack setup that includes measurements for input and output DC voltage and current and power readout. The rack also includes a 1 kW DC HP 6032A system power supply 0-60v/0-50A 1000W (Hewlett-Packard, P.O. Box 58199, Santa Clara, California), which was used to test the DC case. The gating signals were monitored for signal integrity. They are presented and exhibit no distortion. The frequency of the PWM signal was also varied in the range of 5 kHz to 50 kHz. This was achieved by using a capacitor decade box attached to the 555 timer counter chip output, therefore changing the output capacitance and controlling the timer/counter frequency. The optimum

frequency for efficiency is 15 kHz, where efficiency was 40%. The efficiency at 50 kHz was approximately 14%. The reason for the reduced efficiency at higher frequency is added switching losses that are directly proportional to frequency. It is suggested that, in future designs, an alternate switching methodology be adopted to maintain high efficiency. This was verified for both the DC and AC cases. In this scheme, one of the transistors in the bi-directional pair would be switched off when it is reverse biased. This would involve adding two drivers for the two extra transistors and is already available in the circuit. For example, in the positive input voltage DC case the first switch will be driven by PWM and the second switch will be turned off (hard off by connecting its base to -5V). In the output switch pair the second switch will be permanently turned on (hard ON by connecting the base to +15V) and the first switch will be turned off resulting in the self-commutation of the intrinsic diode of the IGBT. This seemingly simple idea of only switching on one transistor results in dramatic improvement in efficiency. Efficiency typically improved from around 15-20% to around 75-90% and is attributed to reduced losses in switching. This scheme was tested by attaching a switch across the bases of the transistors. In future designs this can be implemented by switching each driver on command ON and OFF as needed and as dictated by the phase of the input AC signal. Waveforms are given for each case. Using unipolar switching, very few output spikes are noticed, which is another improvement over bipolar switching.

The full set of output, input, and gating signals are in Appendix D. These were recorded using a Tektronix 11401 digitizing oscilloscope (Tektronix, 26600 SW Parkway,

P.O. Box 1000, Wilsonville, Oregon) equipped with an Tektronix 11A83 differential amplifier for differential measurements.

The voltage waveform is given for the 25%, 50%, and 75% duty cycle. By looking at the output signals we can see the input and output superimposed. At d = 0.25 the converter acts as a buck converter and $\frac{V_O}{V_I} = \frac{D}{1-D} = \frac{0.25}{1-0.25} = \frac{1}{3}$. At d = 0.75 the converter acts as a boost converter and $\frac{V_O}{V_I} = \frac{D}{1-D} = \frac{0.75}{1-0.75} = 3$. At d = 0.5 the converter acts as a 1:1 converter and $\frac{V_O}{V_I} = \frac{D}{1-D} = \frac{0.5}{1-0.5} = 1$. The inductor current and voltage are also presented. The current is triangular and riding on a pedestal indicating that the converter is operated in the continuous current mode.

The experimental results also included the elimination of high-voltage spikes on the output. This was achieved by adding high-frequency capacitors ($4 \times 0.47\ \mu f$). Optimization of the blanking and switch overlapping was found to offer little or no improvement to the output voltage.

6. CONCLUSION

The concept of an electronic transformer was proven to be feasible. It can buck and boost voltage at different duty ratios and can be expanded (if the loop is closed) to provide superior load and line regulation. Line regulation is the immunity of the solid state transformer to abrupt changes in line voltage. In other words, the output is not affected by the abrupt changes in input and maintains regulation. It can also provide load regulation or output regulation. The output voltage is not affected by load changes. So, the solid state transformer becomes load independent. Load changes do not affect the quality of the output signal and do not affect the stability of the closed-loop system. These features are proven in control design and are verified by using Matlab simulation of the closed-loop system. Extensive testing of the closed-loop system will be the ultimate check to verify these results.

The efficiency figures were very promising (85-90%) and more research and experimentation can even improve the efficiency of the transformer to the 95% efficiency level typical in converter designs. This can be achieved by optimizing different parts of the circuit (switches, inductor, capacitor).

The solid state transformer is expected to have a wide range of application in both industry and power distribution (e.g., replacing bulky line transformers with compact, efficient solid state modules). These modules are expandable and offer a wider range of operational voltages and currents. Further development in the field of closed-loop

performance optimization can be attained by fine tuning the circuit parameters. The solid state transformer can later be manufactured in chip form offering a solution to system problems because of its reduced size, more efficient performance, and wider range of input and output voltages. The solid state transformer can replace the variable turns ratio transformer, or load tap changer, with increased dynamic behavior. Another application might be that of a variable AC regulator used as a high-power light dimmer. This can decrease the noise associated with present dimmers, which use silicon controlled rectifier based electronics to waveshape the input signal.

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APPENDIX A

STATE-SPACE DERIVATION

Steps of deriving the transfer function using state-space averaging method

are:

1. Write state equations for the converter (in general) in terms of the state variables for the ON and OFF states of the switches.

2. Average the two equations and multiply by D and (1 - D), which are the ON and OFF times of the switches, respectively.

3. Ignore all the nonlinear terms.

4. Introduce a perturbation to the states of the system and input and output to get the small signal response.

5. Take Laplace transform of the equations to get the closed-form expression

6. Calculate the A,B,C,D matrices for each converter type by modeling the converter in state-space form. The states are the current in the inductor and the voltage across the capacitor.

The following is a detailed explanation and walk through of the derivation.

$$\dot{x} = A_1 x + B_1 v_i \tag{A-1}$$

$$v_o = C_1^T x$$

$$\dot{x} = A_2 x + B_2 v_i \tag{A-2}$$

$$v_o = C_2^T x$$

Multiply A-1 by d and A-2 by (1-d) and add them

$$\dot{x} = (dA_1 + (1-D)A_2)x + (dB_1 + (1-d)B_2)v_i$$

$$\dot{x} = A x + B v_i$$

$$v_o = (d C_1^T + (1-d) C_2^T)x = C^T x$$

$$A = dA_1 + (1-d)A_2$$

$$B = dB_1 + (1-d)B_2$$

$$C^T = dC_1^T + (1-d)C_2^T$$

Let

$$x = X + \hat{x}$$

$$v_i = V_i + \hat{v}_i$$

$$v_o = V_o + \hat{v}_o$$

$$d = D + \hat{d}$$

$$d_o = (1-d)$$

$$d_o = D_o - \hat{d}$$

Thus

$$d + d_o = D + D_o = 1$$

X, V_i, V_o, D, D_o are the steady state values

then

$$\mathbf{X^{\bullet}} = \mathbf{V_i^{\bullet}} = 0$$

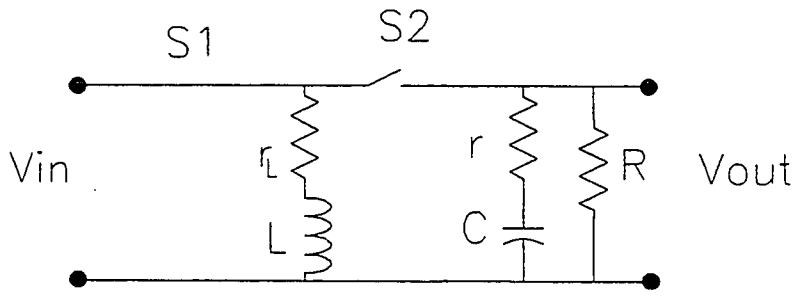


Figure A-1: Buck-Boost converter with S1 ON and S2 OFF.

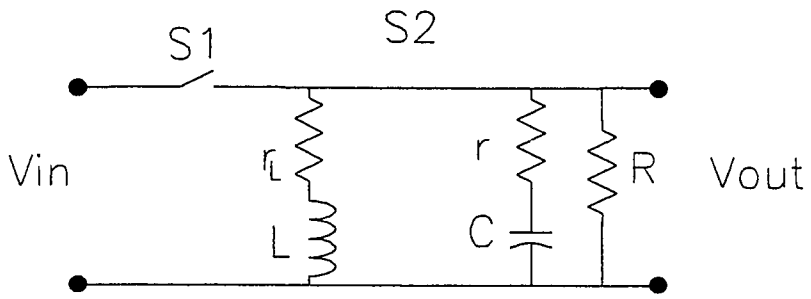


Figure A-2: Buck-Boost converter with S1 OFF and S2 ON.

$$\hat{x}^{\bullet} = \left\{(D+\hat{d})A + (D_o-\hat{d})A_2\right\}(X+\hat{x}) + \left\{(D+\hat{d})B_1 + (D_o-\hat{d})B_2\right\}(V_i+\hat{v}_i)$$

$$\hat{x}^{\bullet} = (DA_1 + D_oA_2)X + (DB_1 + D_oB_2)V_i + (DA_1 + D_oA_2)\hat{x} + (DB_1 + D_oB_2)\hat{v}_i$$
$$+\left[(A_1 - A_2)X + (B_1 - B_2)V_i\right]\hat{d} + \textit{Nonlinear terms}$$

$$\hat{x}^{\bullet} = (AX + BV_i) + (A\hat{x} + B\hat{v}_i) + [(A_1 - A_2)X + (B_1 - B_2)V_i]\hat{d}$$

$$AX + BV_i = 0$$

$$\hat{x}^{\bullet} = (A\hat{x} + B\hat{v}_i) + [(A_1 - A_2)X + (B_1 - B_2)V_i]\hat{d}$$

$$\mathrm{v}_o = V_o + \hat{v}_o = [(D + \hat{d})C_1^T + (D_o - \hat{d})C_2^T](X + \hat{x})$$

$$\mathrm{v}_o = (DC_1^T + D_oC_2^T)X + (DC_1^T + D_oC_2^T)\hat{x} + (C_1^T - C_2^T)X\hat{d} + \textit{Nonlinear terms}$$

$$V_O = C^T X$$

$$\hat{v}_o = C^T\hat{x} + (C_1^T - C_2^T)X\hat{d}$$

$$V_O = C^T X = -C^T A^{-1} BV_i$$

$$\frac{V_o}{V_i} = -C^T A^{-1} B$$

Taking the Laplace transform of $\frac{V_o}{V_i}$

$$\frac{V_o}{V_i} = C^T(SI - A)^{-1} B \qquad \text{(A-3)}$$

By taking the Laplace transform of $\hat{\mathrm{v}}_o$ and $\hat{\mathrm{x}}^{\bullet}$ equations

$$\hat{v}_o = C^T\hat{x} + (C_1^T - C_2^T)X\hat{d}$$

$$\hat{x}^{\bullet} = (A\hat{x} + B\hat{v}_i) + [(A_1 - A_2)X + (B_1 - B_2)V_i]\hat{d}$$

While setting $\hat{v}_i = 0$ to get the $\frac{\hat{v}_o}{\hat{d}}$

$$\frac{\hat{x}}{\hat{d}} = (SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_i]$$

$$\frac{\hat{v}_o}{\hat{d}} = C^T(SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_i] + (C_1^T - C_2^T)X \qquad \text{(A-4)}$$

While setting $\hat{d} = 0$ to get the $\frac{\hat{v}_o}{\hat{v}_i}$

$$\frac{\hat{x}(S)}{\hat{v}_i(s)} = (SI - A)^{-1}B \qquad \text{(A-5)}$$

Equations A-3, A-4, A-5 represent the foundation of the state-space representation. Equation A-3 gives the DC relationship between the input and output. Equation A-4 gives the relationship or transfer function of output voltage with respect to duty cycle or control. Equation 5 gives the transfer function and relationship between input and output in the general case and this is the equation used for the AC case together with Equation A-4 for control design purposes.

For Figure A-1: S1 is closed (ON), S2 is open (OFF) and

$$V_i = r_L i_L + L\frac{di_L}{dt}$$

$$C\frac{dV}{dt} = -\frac{V}{R}$$

$$V_o = -V$$

So

$$A_1 = \begin{bmatrix} \frac{-r_L}{L} & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_i$$

$$C_1^T = \begin{bmatrix} 0 & -1 \end{bmatrix} \begin{bmatrix} i_L \\ V \end{bmatrix}$$

For Figure A-2: S2 is closed (ON), S1 is open (OFF) and:

$$i_L = C\frac{dV}{dt} + \frac{V}{R}$$

$$0 = r_L i_L + L\frac{di_L}{dt} - V$$

$$V_o = r(i_L + \frac{V}{R})$$

So

$$A_2 = \begin{bmatrix} \frac{-r_L}{L} & \frac{1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ V \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i$$

$$C_2^T = \begin{bmatrix} r & \frac{V}{R} \end{bmatrix} \begin{bmatrix} i_L \\ V \end{bmatrix}$$

By using these matrices the transfer functions for the Buck-Boost converter, which are listed below, can be easily calculated.

Where:

C is the converter capacitance

C_L is the load capacitance in the case of inductive loading.

R is the load resistance in case of resistive loading.

r_L is the converter inductor associated resistance.

r is the converter capacitance associated ESR.

I_L is the converter inductor current.

I_{LL} is the load inductance current in the case of inductive loading.

L is the converter inductance.

D is the duty cycle.

Buck-Boost with R load:

$$\frac{V_o}{V_i} = \frac{D_o}{1-D_o} * \frac{1}{LC} \frac{rsC + \frac{r}{R} + 1}{s^2 + \left[\frac{\frac{r_L}{D_o^2} + \frac{r}{D_o}}{L} + \frac{1}{RC}\right] + \frac{\frac{r_L}{D_o^2} + \frac{r}{D_o}}{L} + \frac{1}{LC}}$$

Buck-Boost with L load:

$$\frac{V_o}{V_i} = \frac{D}{LC} \frac{rsC(1-B) - DB - (1-D)(1-CB)}{s^2 + \frac{r_L}{L}s + \frac{(1-D)[DB + (1-D)(1-CB)]}{LC}}$$

where $B = \frac{I_{LL}}{I_L}$

Buck-Boost with C load:

$$\frac{V_o}{V_i} = \frac{D}{LC} \frac{rsC - \frac{1-D}{1+A}}{s^2 + \frac{r_L}{L}s + \frac{(1-D)^2}{(1+A)LC}}$$

where $A = \frac{C_L}{C}$

Output to control transfer function is:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_o}{D_o(1-D_o)}\left[1 - \frac{SDL}{R(1-D_o)^2}\right] H_e(S)$$

where

$$H_e(s) = \frac{1}{LC} \frac{rsC + \frac{r}{R} + 1}{s^2 + \left[\frac{\frac{r_L}{D_o^2} + \frac{r}{D_o}}{L} + \frac{1}{RC} \right] + \frac{\frac{r_L}{D_o^2} + \frac{r}{D_o}}{L} + \frac{1}{LC}}$$

APPENDIX B

MAGNETICS DESIGN AND DRIVER CIRCUITS

This appendix discusses the design of the magnetic circuit. This includes the choice of L, wire size, core type, and air-gap size. Included are circuit diagrams for the driver circuit, the power supply circuit, and the PWM circuit.

For the design of the magnetic circuit 50% duty cycle was used and:

$$V_L = L\frac{di}{dt} = 1.41 * 120Vrms = 170Vpeak$$

$$\frac{di}{dt} = \frac{20A}{10\mu S}$$

$$L = \frac{170 * 10}{20} = 85\mu H$$

$$I_{LBoundary} = \frac{I_{LPEAK}}{2} = \frac{20}{2} = 10A$$

$$I_L = \frac{T_S * V_{in} * D}{2 * L}$$

$$\text{Minimum L} = \frac{20\mu * 170 * 0.5}{2 * 10}$$

$$\text{Minimum L} = 85\mu H$$

Two cores were used and L was chosen to be 100 μ H, so for each core L is equal to 50 μH.

$LI^2 = (50\mu H)(20A)^2 = 20mJ$

From charts for EC cores, the EC-70D-47035 was chosen, which corresponds to

$$A_L = \frac{L}{N^2} = \frac{50\mu}{N^2} = 160 \text{ mH} / 1000 \text{ turns}$$

$$A_L = \frac{160m}{(1000)^2} = \frac{160nH}{T^2}$$

$$L = N^2 * A_L$$

$$50\mu = N^2 * (160nH)$$

$$N = \sqrt{\frac{50 * 10^{-6}}{160 * 10^{-9}}} = 17.67$$

$$N \cong 18 \text{ turns.}$$

The air gap is approximately 0.03 inches and was selected from the chart of A_L versus the gap on the EC-70 core.

The wire used:

$$I = 20A$$

$$I_{RMS} = 20 * (0.707) = 14.14A$$

Size of wire AWG @500cir Mils / Amp

AWG = (14.14) * (500) = 7,071 Cir Mils

In figure 12

#13 < AWG < #12

5,852 7,310

AWG = #12

Always choose the smaller table.

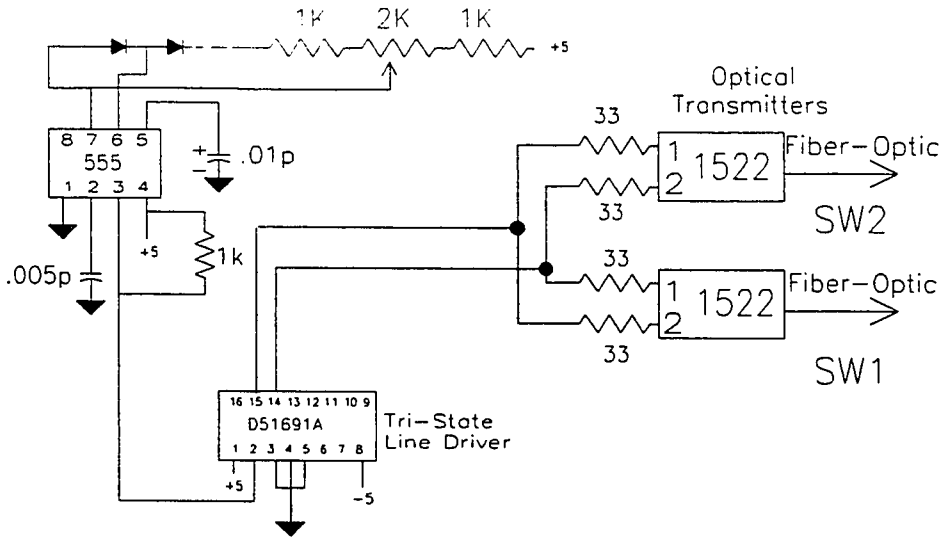


Figure B-1: PWM circuit design using 555 timer/counter chip. The circuit also employs the 51891A tri-state line driver to transmit the signal to the 1522 optical transmitters across the fiber optic cables to the gate drivers for SW1 and SW2. (The complete IC data sheets are presented in Appendix C.)

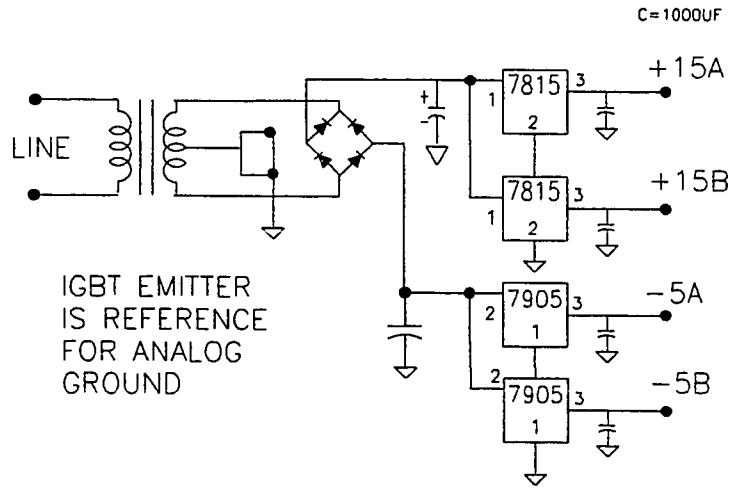


Figure B-2: Power supply for the driver boards. The circuit employs a center-tapped transformer, a diode bridge, and the 7815 and 7905 +15 and -5 voltage regulators.

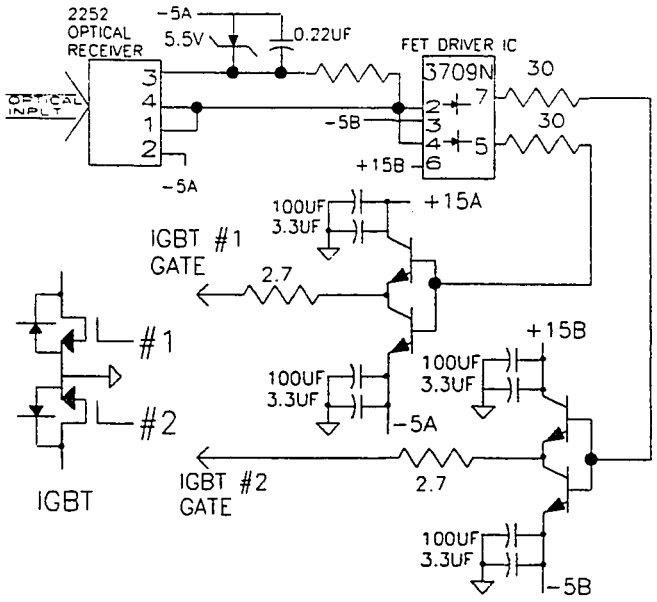


Figure B-3: Gate driver board. The circuit employs the 2252 optical receiver, the field-effect transistor (FET) driver IC 3709, and the emitter follower configuration.

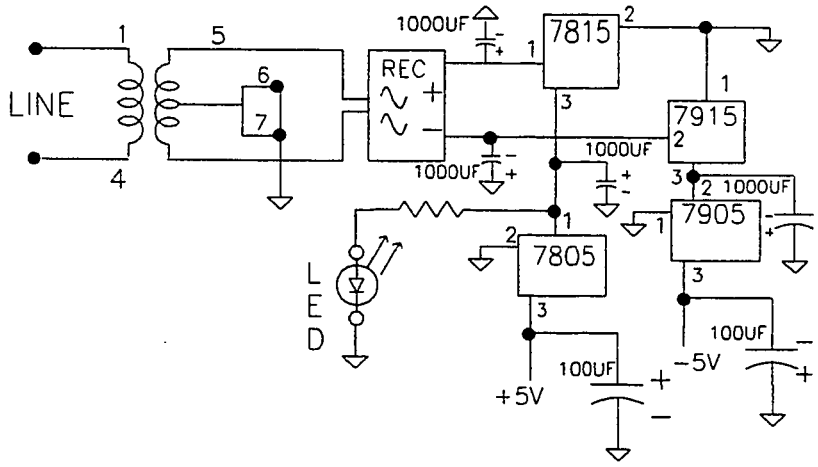


Figure B-4: Power supply for the whole circuit. The circuit employs a cente- tap transformer, a diode rectifier bridge, 7815/7915/7805/7905 linear regulators, and a light-emitting diode (LED) used as an indicator.

Wire Tables

Table 5 — Magnet Wire

Wire Size AWG	Wire Area (Max.)* Heavy Circular Mils	Wire Area (Max.)* Heavy $cm^2 10^{-3}$	Turns** per in^2	Turns** per cm^2	Resistance Ohms/1000'	Current Capacity (ma) @750 Cir. Mil/amp	Current Capacity (ma) @500 Cir. Mil/amp
10	11,470	58.13	89	13.8	.9987	13,840	20,768
11	9,158	46.42	112	17.4	1.261	10,968	16,452
12	7,310	37.05	140	21.7	1.588	8,705	13,058
13	5,852	29.66	176	27.3	2.001	6,912	10,368
14	4,679	23.72	220	34.1	2.524	5,478	8,220
15	3,758	19.05	260	40.3	3.181	4,347	6,520
16	3,003	15.22	330	51.2	4.020	3,441	5,160
17	2,421	12.27	410	63.6	5.054	2,736	4,100
18	1,936	9.812	510	79.1	6.386	2,165	3,250
19	1,560	7.907	635	98.4	8.046	1,719	2,580
20	1,246	6.315	800	124	10.13	1,365	2,050
21	1,005	5.094	1,000	155	12.77	1,083	1,630
22	807	4.090	1,200	186	16.20	853	1,280
23	650	3.294	1,500	232	20.30	681	1,020
24	524	2.656	1,900	294	25.67	539	808
25	424	2.149	2,400	372	32.37	427	641
26	342	1.733	3,000	465	41.0	338	506
27	272	1.379	3,600	558	51.4	259	403
28	219	1.110	4,700	728	65.3	212	318
29	180	0.9123	5,600	868	81.2	171	255
30	144	0.7298	7,000	1,085	104	133	200
31	117	0.5930	8,500	1,317	131	106	158
32	96.0	0.4866	10,500	1,628	162	85	128
33	77.4	0.3923	13,000	2,015	206	67	101
34	60.8	0.3082	16,000	2,480	261	53	79
35	49.0	0.2484	20,000	3,100	331	42	63
36	39.7	0.2012	25,000	3,876	415	33	50
37	32.5	0.1647	32,000	4,961	512	27	41
38	26.0	0.1318	37,000	5,736	648	21	32
39	20.2	0.1024	50,000	7,752	847	16	25
40	16.0	0.0811	65,000	10,077	1,080	13	19
41	13.0	0.0659	80,000	12,403	1,320	11	16
42	10.2	0.0517	100,000	15,504	1,660	8.5	13
43	8.40	0.0426	125,000	19,380	2,140	6.5	10
44	7.30	0.037	150,000	23,256	2,590	5.5	8
45	5.30	0.0269	185,000	28,682	3,348	4.1	6.2

Table 6 — Litz Wire

Litz Wire Size	Turns*** per in^2	Turns*** per cm^2
5/44	28,000	4,341
6/44	25,000	3,876
7/44	22,000	3,410
12/44	13,000	2,016
20/44	7,400	1,147
30/44	4,000	620
40/44	3,000	465
50/44	2,300	356
60/44	1,900	294

Litz Wire Size	Turns*** per in^2	Turns*** per cm^2
72/44	1,500	232
80/44	1,400	217
90/44	1,200	186
100/44	1,100	170
120/44	900	140
150/44	700	108
180/44	500	77
360/44	250	38

*Areas are for maximum wire area plus maximum insulation buildup.

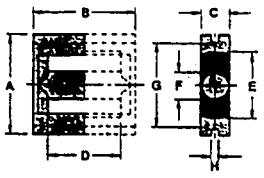
**Based on a typical machine layer wound coil.

***Based on a typical layer wound coil.

Table B-1: Wire size selection tables (Magnetics ref. 20).

Section 12.

EC Cores



PHYSICAL DIMENSIONS

PART NUMBER	TYPE		A	B	C & F	D	E	G	H
*-43517-EC	(EC35)	in.	1.358 ± .030	1.362 ± .012	.374 ± .012	.938 min.	.8955 ± .020	1.122 ± .030	.108 ± .010
		mm.	34.49	34.6			22.75	28.50	
*-44119-EC	(EC41)	in.	1.600 ± .035	1.536 ± .012	.457 ± .012	1.062 min.	1.065 ± .030	1.322 ± .036	.128 ± .010
		mm.	40.64	39.02			27.06	33.58	
*-45224-EC	(EC52)	in.	2.055 ± .050	1.906 ± .012	.5275 ± .013	1.22 min.	1.300 ± .035	1.732 ± .060	.1475 ± .009
		mm.	52.20	48.42			33.02	43.99	
*-47035-EC	(EC70)	in.	2.756 ± .060	2.716 ± .012	.645 ± .015	1.758 min.	1.762 ± .045	2.346 ± .060	.187 ± .010
		mm.	70.00	68.98			44.50	59.60	

MAGNETIC DATA

PART NUMBER	Ungapped A_L mH/1000 turns			Magnetic Path Length (cm)	Core Area (cm^2)	Minimum Core Area (cm^2)	Core Volume (cm^3)	Set Nom. Weight (gms)	WaAc (cm^4) (note 1)
	R (min.)	P (min.)	F (±25%)						
*-43517-EC	1660	1800	3000	7.59	.858	.709	6.52	38	.833
*-44119-EC	2210	2400	3700	8.76	1.24	1.06	10.9	62	1.67
*-45224-EC	2800	3150	5040	10.3	1.82	1.41	18.6	111	3.87
*-47035-EC	3310	3600	5760	14.1	2.61	2.11	38.6	253	13.4

* Add material code to order correct part number.

(1) Product of window area and core area.

HOW TO ORDER: (a) Add (*) material code to part number.
(b) If center leg is to be gapped, specify gap size, and H in one piece or both/set.
(c) Cores are sold in pieces. Gapped pieces are normally packed seperately from ungapped pieces. If desired in sets, this must be specified.

FOR PREFERRED PARTS, SEE INSIDE BACK COVER

STANDARD GAPPED EC CORES

Type	(P Material) Part No. Combination*	Approx. A_L	μe	Total Gap
EC 35	P-43517-EC-00 and (one of each) P-43517-EC-02	115	73	.047 ± .001"
	P-43517-EC-02 (two each)	68	43	.094 ± .002"
EC41	P-44119-EC-00 and (one of each) P44119-EC-02	100	56	.086 ± .001"
	P-44119-EC-02 (two each)	57	33	.172 ± .002"
EC52	P-45224-EC-00 and (one of each) P-45224-EC-02	195	92	.048 ± .001"
	P-45224-EC-02 (two each)	112	53	.098 ± .002"
EC70	P-47035-EC-00 and (one of each) P-47035-EC-02	200	82	.076 ± .001"
	P-47035-EC-02 (two each)	117	48	.150 ± .002"

*Also available in F, K, and R materials. Substitute material code in part number. E.g., F-43517-EC-00.

GAP vs. A_L

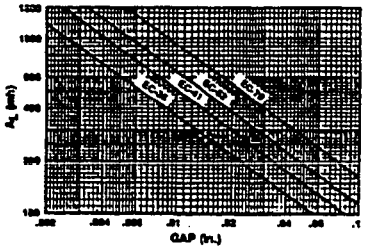


Table B-2: Air gap selection tables (Magnetics ref. 20).

Ferrite DC Bias Core Selector Charts

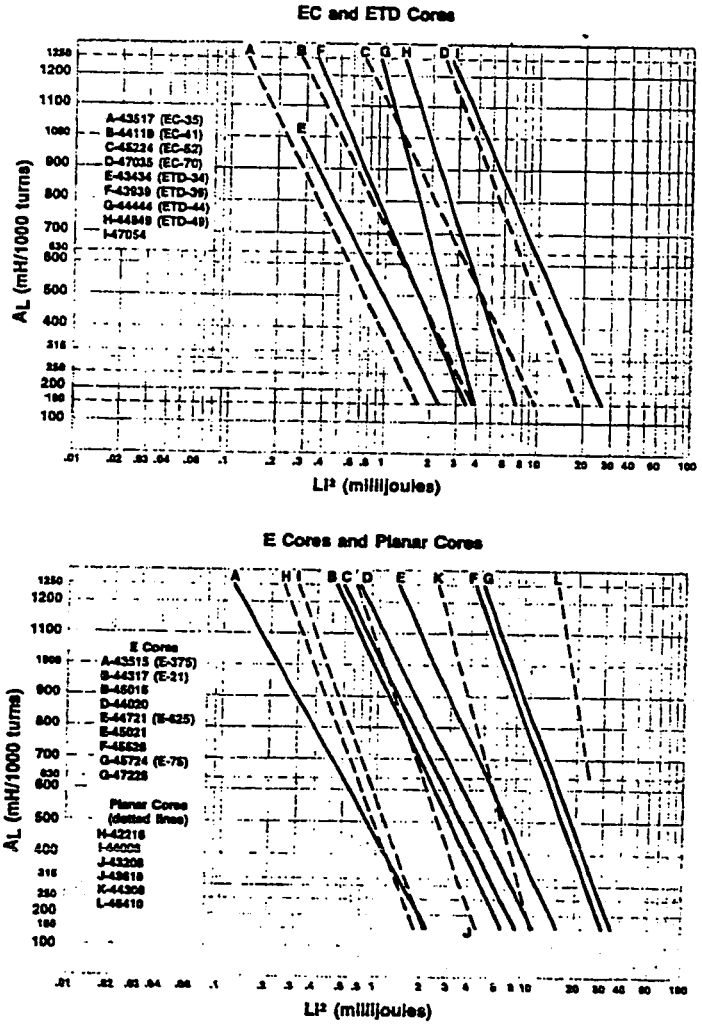


Table B-3: Magnetic core selection charts (Magnetics ref. 20).

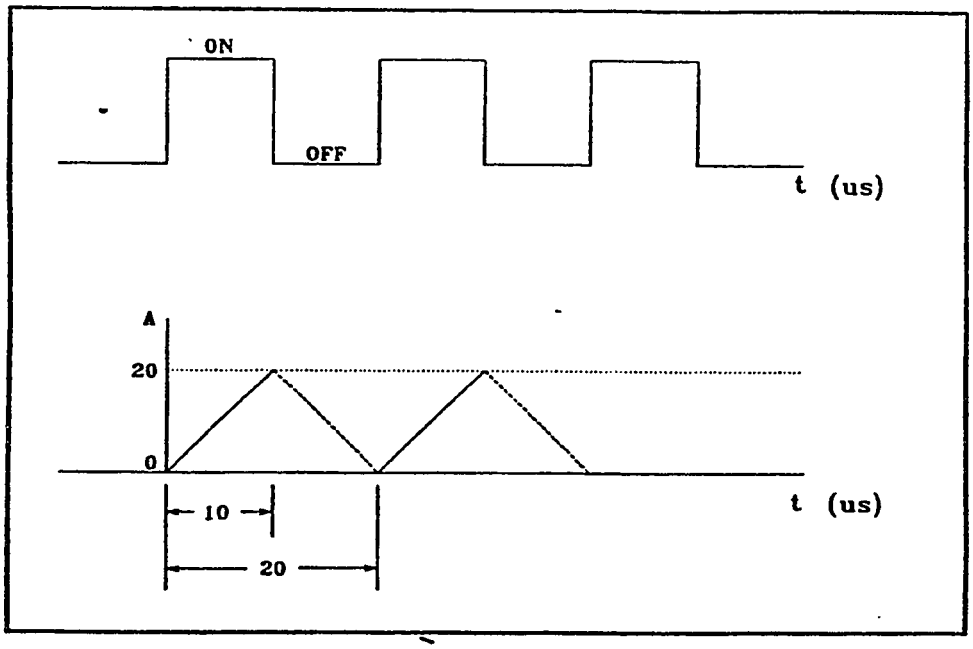


Figure B-5: Inductor current timing waveform.

APPENDIX C

COMPONENT DATA SHEETS

This appendix includes all the components used in this design. The key ratings of the components are:

1. MG400Q1Us11 IGBT MOSFET (Toshiba).

   Ratings: 1200V collector-emitter voltage, and 800A forward current.

2. D44H NPN Complementary silicon power transistor (Motorola).

   Rating: 80V collector-emitter voltage, and 20A collector current.

3. UC3709 dual high speed FET driver (Unitrode).

   Rating: 1.5A source/sink drive, 5-40V output swing.

4. MC7800 series positive voltage regulator (Motorola).

   Rating: Output current 1A, MC7805/7815 offers 5V/15V regulated output.

5. MC7900 Negative voltage regulator (Motorola).

   Rating: Output current 1A, MC7905/7915 offers 5V/15V regulated output.

6. DS1691A tri-state line driver (National Semiconductor).

7. HFBR1522/2522 fiber optic link system. Includes transmitter, receiver, and fiber optic cables (Hewlett Packard).

Rating: High performance 1 megabit per second non-return to zero (NRZ) transmission/reception. Allows up to 24 meters of cable link length. Propagation delay of 180ns (typical).

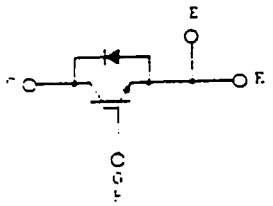
SILICON N CHANNEL IGBT

MG400Q1US11
MG400Q1US21

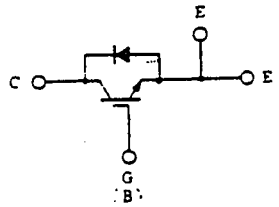
HIGH POWER SWITCHING APPLICATIONS.
MOTOR CONTROL APPLICATIONS.

- High Input Impedance
- High Speed : tf=1.0μs(Max.), trr=0.5μs(Max.)
- Low Saturation Voltage : VCE(sat)=2.7V(Max.)
- Enhancement-Mode
- The Electrodes are Isolated from Case.

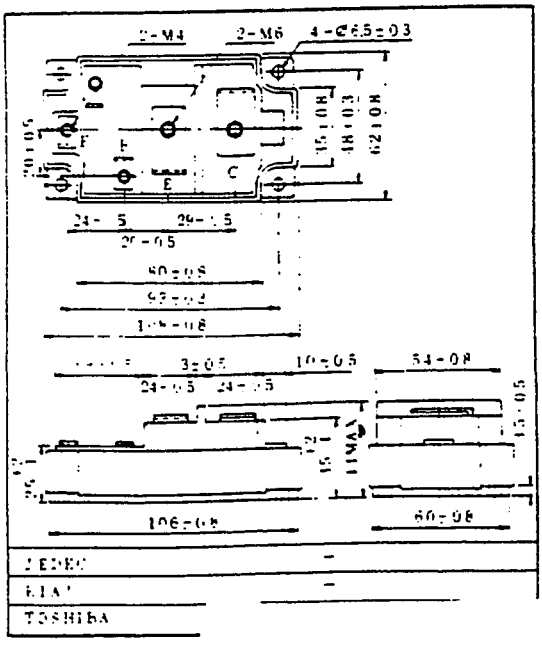
EQUIVALENT CIRCUIT (MG400Q1US11)



EQUIVALENT CIRCUIT (MG400Q1US21)



Unit in mm



Unit in mm

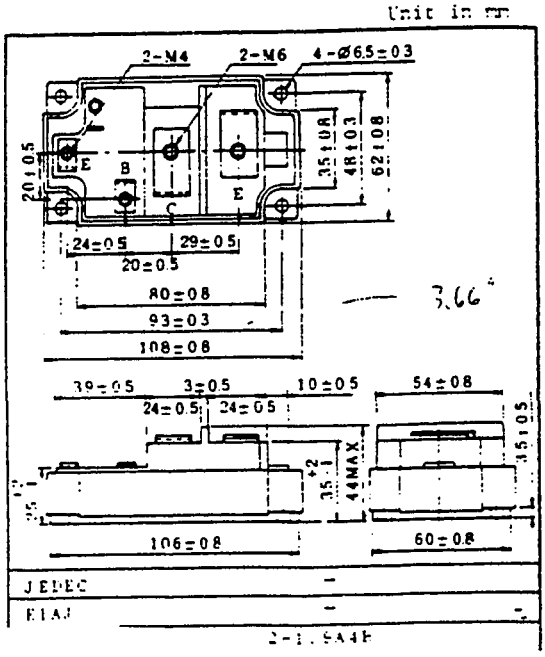


Figure C-1: IGBT MOSFET data sheet (Toshiba ref. 21).

MG400Q1US11
MG400Q1US21

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	1200	V
Gate-Emitter Voltage		V_{GES}	±20	V
Collector Current	DC	I_C	400	A
	1ms	I_{CP}	800	
Forward Current	DC	I_F	400	A
	1ms	I_{FM}	800	
Collector Power Dissipation (Tc=25°C)		P_C	1600	W
Junction Temperature		Tj	150	°C
Storage Temperature Range		Tstg	−40~125	°C
Isolation Voltage		VIsol	2500 (AC, 1 minute)	V
Screw Torque (Terminal M4/M6/Mounting)		−	2/3/3	N·m

ELECTRICAL CHARACTERISTICS (Ta=25°C)

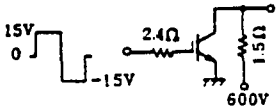
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.
Gate Leakage Current		I_{GES}	V_{GE}=±20V, V_{CE}=0	−	−	±500
Collector Cut-off Current		I_{CES}	V_{CE}=1200V, V_{GE}=0	−	−	−
Collector-Emitter Breakdown Voltage		$V_{(BR)CES}$	I_C=4mA, V_{GE}=0	1200	−	−
Gate-Emitter Cut-off Voltage		$V_{GE(OFF)}$	I_C=400mA, V_{CE}=5V	3.0	−	6.5
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=400A, V_{GE}=15V	−	2.2	2.7
Input Capacitance		Cies	V_{CE}=10V, V_{GE}=0, f=1MHz	−	59000	−
Switching Time	Rise Time	t_r		−	0.3	0.5
	Turn-on Time	t_{on}		−	0.4	0.8
	Fall Time	t_f		−	0.6	1.2
	Turn-off Time	t_{off}		−	1.2	1.8
Forward Voltage		V_F	I_F=400A, V_{GE}=0	−	2.0	3.0
Reverse Recovery Time		t_{rr}	I_F=400A, V_{GE}=−10V di/dt=300A/μs	−	0.25	0.5
Thermal Resistance		$R_{th(j-c)}$	Transistor	−	−	0.08
			Diode	−	−	0.2

Figure C-1 (concluded): IGBT MOSFET data sheet (Toshiba).

NPN
D44H Series
PNP
D45H Series

MOTOROLA

1.3

COMPLEMENTARY SILICON POWER TRANSISTORS

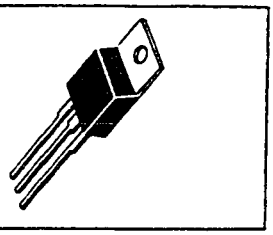
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

30-80 VOLTS



MAXIMUM RATINGS

Rating	Symbol	D44H or D45H				Unit
		1,2	4,5	7,8	10,11	
Collector-Emitter Voltage	V_{CEO}	30	45	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak (1)	I_C	10 20				Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	50 1.67				Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150				°C

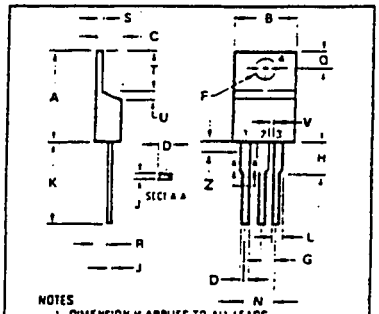
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 5.0 ms, Duty Cycle ≤ 50%

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	D44H1,4,7,10 D45H1,4,7,10	h_{FE}	35	—	—
	D44H2,5,8,11 D45H2,5,8,11		60	—	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H1,4,7,10 D45H1,4,7,10		20	—	
	D44H2,5,8,11 D45H2,5,8,11		40	—	



NOTES
1. DIMENSION H APPLIES TO ALL LEADS
2. DIMENSION L APPLIES TO LEADS 1 AND 3
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
5. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	-	0.045	-
Z	-	2.03	-	0.080

STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-02
(TO-220AB)

Figure C-2: Complementary silicon power transistor (Motorola ref. 22).

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	—	—	100	μA
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.4 Adc)	D44H/D45H2,5,8,11	$V_{CE(sat)}$	—	—	1.0	Vdc
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D44H/D45H1,4,7,10		—	—	1.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	D44H Series	C_{cb}	—	130	—	pF
	D45H Series		—	230	—	
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	D44H Series	f_T	—	50	—	MHz
	D45H Series		—	40	—	
SWITCHING TIMES						
Delay and Rise Times (I_C = 5.0 Adc, I_{B1} = 0.5 Adc)	D44H Series	$t_d + t_r$	—	300	—	ns
	D45H Series		—	135	—	
Storage Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	D44H Series	t_s	—	500	—	ns
	D45H Series		—	500	—	
Fall Time (I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	D44H Series	t_f	—	140	—	ns
	D45H Series		—	100	—	

FIGURE 1 — NORMALIZED DC CURRENT GAIN

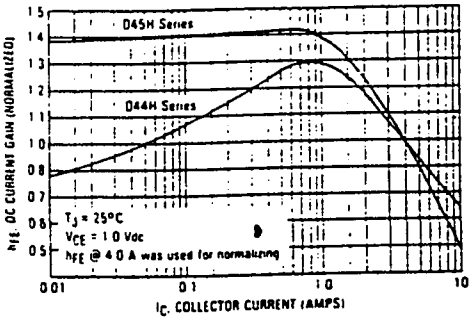


FIGURE 2 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

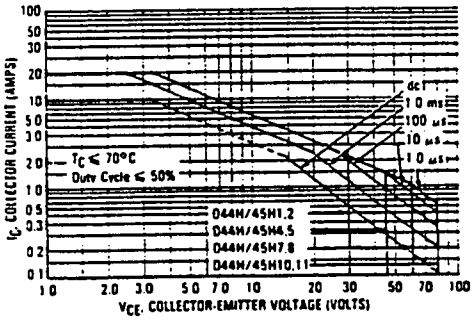


Figure C-2 (concluded): Complementary silicon power transistor (Motorola).

INTEGRATED CIRCUITS
UNITRODE

UC1709
UC3709

Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection
- 8-Pin Minidip Package

DESCRIPTION

The UC1709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 amps of either source or sink current from a totem-pole output stage configured for minimal cross-conduction current spike.

Packaged in an 8-Pin ceramic or plastic minidip, the 1709 (3709) is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30V. This design also includes thermal shutdown protection and an under-voltage lockout circuit which prevents any undefined states at turn-on or turn-off by disabling the output stage.

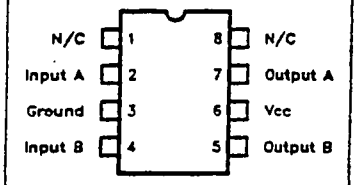
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40V	40V
Output Current (Source or Sink)		
Steady-State	±500 mA	±500 mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20 µJ	15 µJ
Digital Inputs (See Note)	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W
Derate above 50°C	10 mW/°C	10 mW/°C
Power Dissipation at T_C = 25°C	3W	2W
Derate for Case Temperature above 25°C	25 mW/°C	16 mW/°C
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Load Temperature (Soldering, 10 Seconds)	300°C	300°C

Note: All currents are positive into, negative out of the specified terminals. Digital Drive can exceed 5.5V if input current is limited to 10 mA.

CONNECTION DIAGRAM

TOP VIEW
8-PIN N or J PACKAGE



SIMPLIFIED SCHEMATIC (Only One Driver Shown)

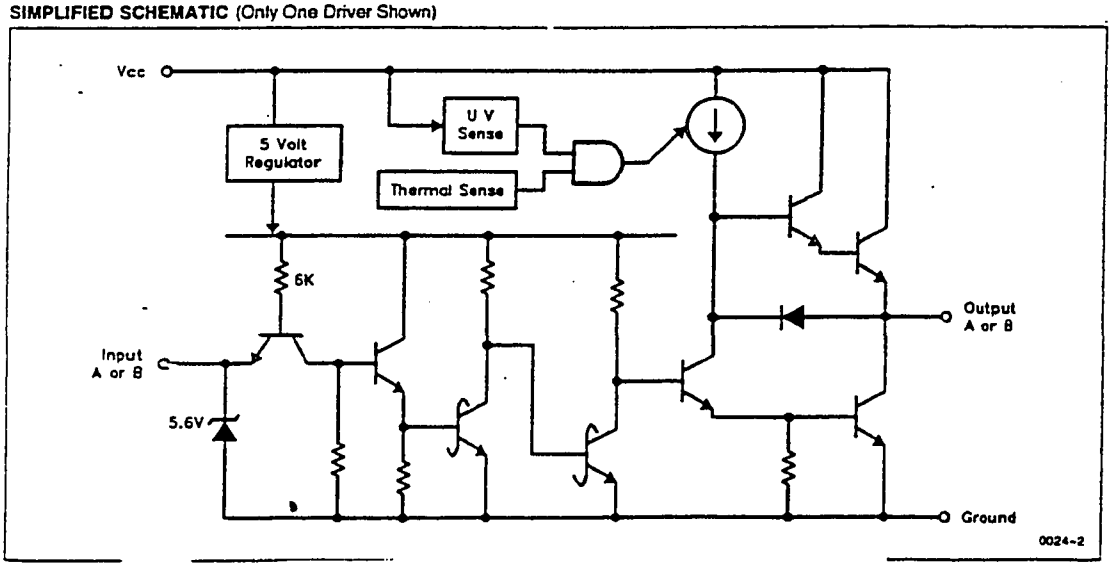


Figure C-3: Dual high-speed FET driver (Unitrode ref. 23).

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, these specifications apply for T_A = −55°C to +125°C for the UC1709, and 0°C to +70°C for the UC3709; V_{CC} = 20V) $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Both Outputs High		10	12	mA
Supply Current	Both Outputs Low		7	10	mA
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_I = 0V		−0.6	−1.0	mA
Input Leakage	V_I = 5V		0.05	0.1	mA
Output High Sat., $V_{CC}-V_O$	I_O = −50 mA		1.5	2.0	V
Output High Sat., $V_{CC}-V_O$	I_O = −500 mA		2.0	2.5	V
Output Low Sat., V_O	I_O = 50 mA		0.1	0.4	V
Output Low Sat., V_O	I_O = 500 mA		2.0	2.5	V
Thermal Shutdown			155		°C

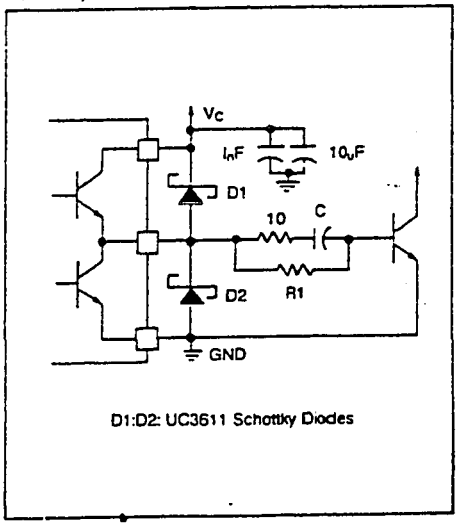
TYPICAL SWITCHING CHARACTERISTICS (V_{CC} = 20V, T_A = 25°C. Delays measured to 10% output change)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =		UNITS
		0 nF	2.2 nF	
Rise Time Delay		80	80	ns
10% to 90% Rise		20	40	ns
Fall Time Delay		60	80	ns
90% to 10% Fall		20	40	ns
V_{CC} Cross Conduction Current Spike	Output Rise	25		ns
	Output Fall	0		ns

NOTE: Refer to UC1705 specification for further information.

APPLICATIONS

Power Bipolar Drive Circuit



Transformer Coupled Push-Pull MOSFET Drive Circuit

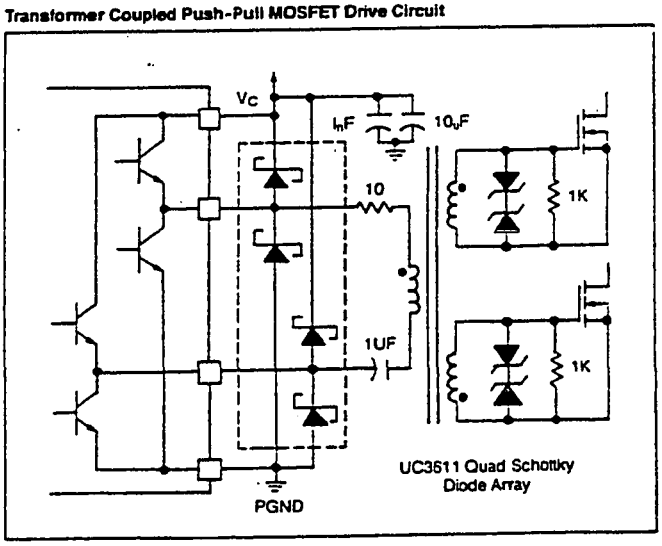
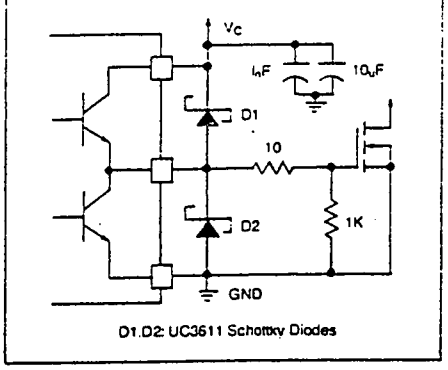


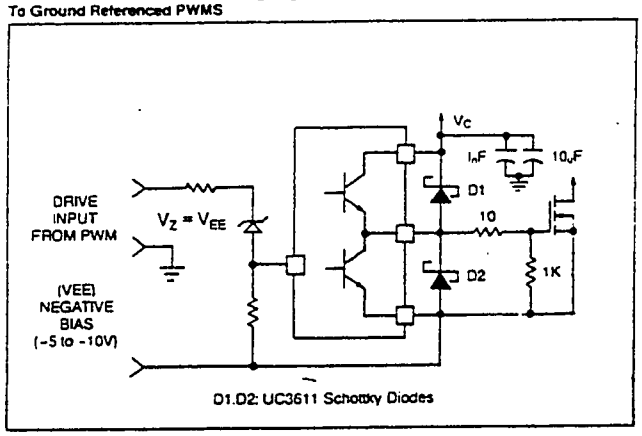
Figure C-3 (continued): Dual high-speed FET driver (Unitrode).

Power MOSFET Drive Circuit



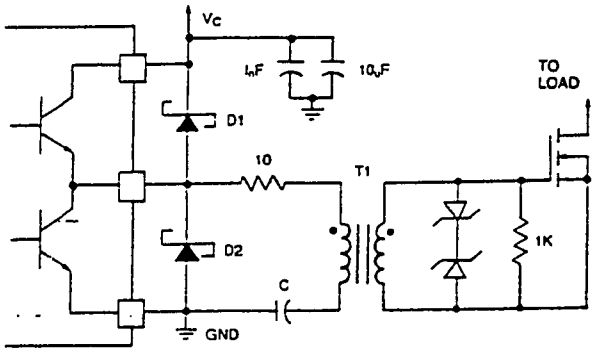
D1,D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS



D1,D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1,D2: UC3611 Schottky Diode Array

Charge Pump Circuits

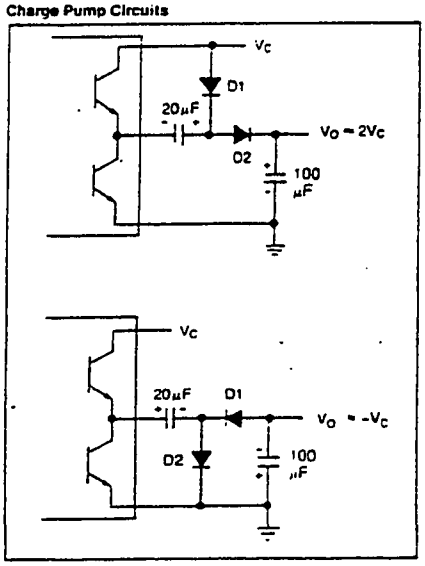


Figure C-3 (concluded): Dual high-speed FET driver (Unitrode).

MOTOROLA

MC7800 Series

THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

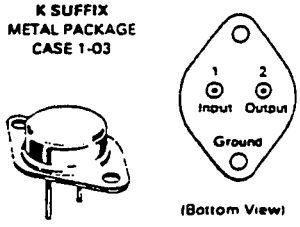
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUITS

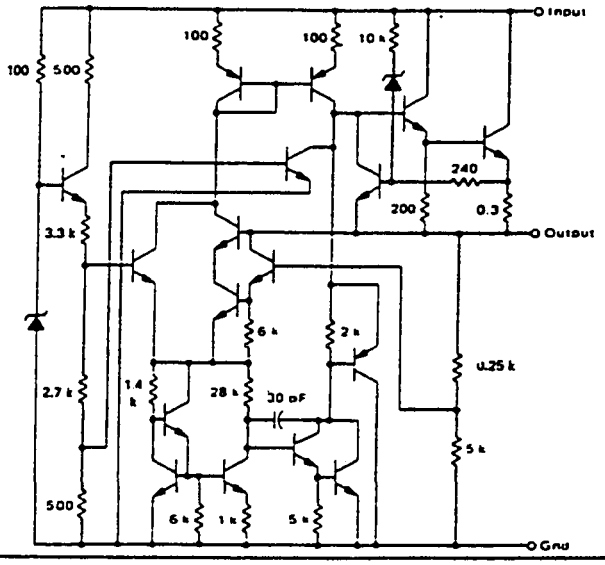
K SUFFIX
METAL PACKAGE
CASE 1-03



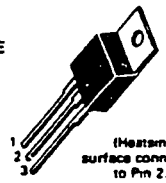
(Bottom View)

Pins 1 and 2 electrically isolated from case. Case is third electrical connection.

REPRESENTATIVE SCHEMATIC DIAGRAM



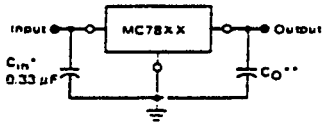
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



PIN 1. INPUT
2. GROUND
3. OUTPUT

(Heatsink surface connected to Pin 2.)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78XXK MC78XXAK*	4% 2%	−55 to +150°C	Metal Power
MC78XXCK MC78XXACK*	4% 2%	0 to +125°C	Metal Power
MC78XXCT MC78XXACT	4% 2%	0 to +125°C	Plastic Power
MC78XXBT	4%	−40 to +125°C	Plastic Power

*2% regulators in Metal Power packages are available in 5, 12 and 15 volt devices.

TYPE NO./VOLTAGE			
MC7805	5.0 Volts	MC7812	12 Volts
MC7806	6.0 Volts	MC7815	15 Volts
MC7808	8.0 Volts	MC7818	18 Volts
MC7809	9.0 Volts	MC7824	24 Volts

Figure C-4: Positive voltage regulator (Motorola ref. 24).

MC7800 Series

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J		°C
MC7800_A		–55 to +150	
MC7800C,AC		0 to +150	
MC7800B		–40 to +150	

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

Figure C-4 (continued): Positive voltage regulator (Motorola).

MC7805, B, C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted).

Characteristic	Symbol	MC7805			MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	— 4.65	— 5.0	— 5.35	— 4.75	— 5.0	— 5.25	4.75 —	5.0 —	5.25 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	— —	2.0 1.0	50 25	— —	7.0 2.0	100 50	— —	7.0 2.0	100 50	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	25 8.0	100 25	— —	40 15	100 50	— —	40 15	100 50	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.2	6.0	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.3 0.5	— — —	— — —	1.3 — 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	68	75	—	—	68	—	—	68	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	$\mu V / V_O$
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	—	-1.1	—	mV/°C

MC7805A, AC

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7805A			MC7805AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C	Reg_{line}	— — — —	2.0 3.0 1.0 2.0	10 10 4.0 10	— — — —	7.0 10 2.0 7.0	50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	25 25 — 8.0	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.2	5.0 4.0	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	68 68	75 75	— —	— —	— 68	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	$\mu V / V_O$
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	17	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±0.6	—	—	-1.1	—	mV/°C

NOTES 1. T_{low} = -55°C for MC78XX, A
= 0° for MC78XXC, AC
= -40°C for MC78XXB
T_{high} = +150°C for MC78XX, A
= +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure C-4 (continued): Positive voltage regulator (Motorola).

MC7815, B, C
ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristic	Symbol	MC7815			MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	— 14.25	— 15	— 15.75	— 14.25	— 15	— 15.75	14.25 —	15 —	15.75 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	— —	60 30	150 75	— —	13 60	300 150	— —	13 60	300 150	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	32 10	150 75	— —	52 20	300 150	— —	52 20	300 150	mV
Quiescent Current (T_J = +25°C)	I_B	—	3.4	6.0	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	— 0.3 0.04	— 0.8 0.5	— — —	— — —	— 1.0 0.5	— — —	— — —	1.0 — 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	60	66	—	—	58	—	—	58	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	—	-1.0	—	mV/°C

MC7815A, AC
ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1] unless otherwise noted)

Characteristics	Symbol	MC7815A			MC7815AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.7	15	15.3	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤ 15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C	Reg_{line}	— — — —	6.0 6.0 3.0 6.0	22 22 10 22	— — — —	13 16 6.0 13	150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— — — —	2.0 2.0 1.0 1.0	25 25 15 25	— — — —	52 52 — 20	100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 3.4	5.5 4.5	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— — —	0.3 0.2 0.04	0.5 0.5 0.2	— — —	— — —	0.8 0.8 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	60 60	66 66	— —	— —	— 58	— —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.0	2.5	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	40	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	—	19	—	mΩ
Short-Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{sc}	—	0.2	1.2	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	1.3	2.5	3.3	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	±1.8	—	—	-1.0	—	mV/°C

NOTES: 1. T_{low} = -55°C for MC78XX, A; T_{high} = +150°C for MC78XX, A
= 0° for MC78XXC, AC = +125°C for MC78XXC, AC, B
= -40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure C-4 (concluded): Positive voltage regulator (Motorola).

MOTOROLA

MC7900 Series

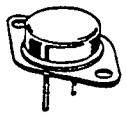
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

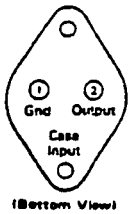
Available in fixed output voltage options from −5.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

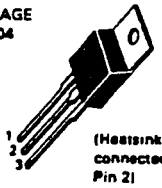


K SUFFIX
METAL PACKAGE
CASE 1-03



(Bottom View)

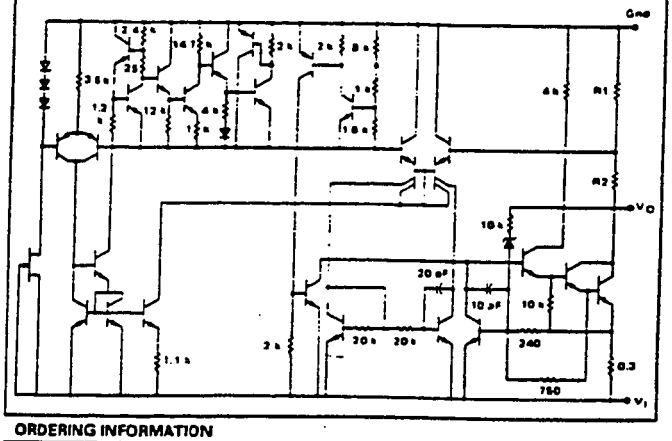
T SUFFIX
PLASTIC PACKAGE
CASE 221A-04



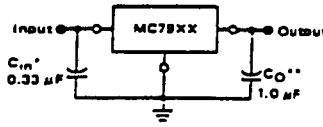
PIN 1. GROUND
2. INPUT
3. OUTPUT

(Heatsink surface connected to Pin 2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC79XXCK	4%	T_J = 0°C to +125°C	Metal Power**
MC79XXACK*	2%		
MC79XXCT	4%		Plastic Power
MC79XXACT*	2%		
MC79XX8T#	4%	T_J = −40°C to +125°C	

XX indicates nominal voltage.
*2% output voltage tolerance available in 5, 12 and 15 volt devices.
**Metal power package available in 5, 12 and 15 volt devices.
#Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 volt devices. Contact your local Motorola sales office for information.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE			
MC7905	5.0 Volts	MC7912	12 Volts
MC7905.2	5.2 Volts	MC7915	15 Volts
MC7906	6.0 Volts	MC7918	18 Volts
MC7908	8.0 Volts	MC7924	24 Volts

Figure C-5: Negative Voltage Regulator (Motorola ref. 24).

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (-5.0 V ≥ V_O ≥ -18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/R_{\theta JA}$	15.4	mW/°C
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +95°C (See Figure 1)	$1/R_{\theta JC}$	200	mW/°C
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/R_{\theta JA}$	22.2	mW/°C
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C	$1/R_{\theta JC}$	182	mW/°C
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	— Plastic Package	$R_{\theta JA}$	65	°C/W
	— Metal Package		45	
Thermal Resistance, Junction to Case	— Plastic Package	$R_{\theta JC}$	5.0	°C/W
	— Metal Package		5.5	

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		—	7.0	50	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		—	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		—	35	100	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		—	8.0	50	
Load Regulation (T_J = +25°C) (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	11	100	
250 mA ≤ I_O ≤ 750 mA		—	4.0	50	
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.75	—	-5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.0 Vdc ≥ V_I ≥ -25 Vdc		—	—	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		—	—	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure C-5 (continued): Negative voltage regulator (Motorola).

MC7905AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.9	-5.0	-5.1	Vdc
Line Regulation (Note 1) -8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A, T_J = 25°C -8.0 Vdc ≥ V_I ≥ -12 Vdc; I_O = 1.0 A -7.5 Vdc ≥ V_I ≥ -25 Vdc; I_O = 500 mA -7.0 Vdc ≥ V_I ≥ -20 Vdc; I_O = 1.0 A, T_J = +25°C	Reg_{line}	— — — —	2.0 7.0 7.0 6.0	25 50 50 50	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	— — —	11 4.0 9.0	100 50 100	mV
Output Voltage -7.5 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.80	—	-5.20	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -7.5 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	— — —	— — —	1.3 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.2 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	— — — —	8.0 2.2 37 8.5	52 27 105 52	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	12 4.5	105 52	mV
Output Voltage -7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-4.95	—	-5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change -7.2 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	— —	— —	1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	42	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	68	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure C-5 (continued): Negative voltage regulator (Motorola).

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) -17.5 Vdc ≥ V_I ≥ -30 Vdc -20 Vdc ≥ V_I ≥ -26 Vdc (T_J = +25°C, I_O = 500 mA) -17.5 Vdc ≥ V_I ≥ -30 Vdc -20 Vdc ≥ V_I ≥ -26 Vdc	Reg_{line}	 — — — —	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 68 25	 300 150	mV
Output Voltage -17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-14.25	—	-15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc ≥ V_I ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

MC7915AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.7	-15	-15.3	Vdc
Line Regulation (Note 1) -20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A, T_J = 25°C -20 Vdc ≥ V_I ≥ -26 Vdc; I_O = 1.0 A. -17.9 Vdc ≥ V_I ≥ -30 Vdc; I_O = 500 mA -17.5 Vdc ≥ V_I ≥ -30 Vdc; I_O = 1.0 A, T_J = 25°C	Reg_{line}	 — — — —	 27 57 57 57	 75 150 150 150	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 68 25 40	 150 75 150	mV
Output Voltage -17.9 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-14.4	—	-15.6	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change -17.5 Vdc ≥ V_I ≥ -30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	-1.0	—	mV/°C

Note:
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure C-5 (concluded): Negative voltage regulator (Motorola).

National Semiconductor

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

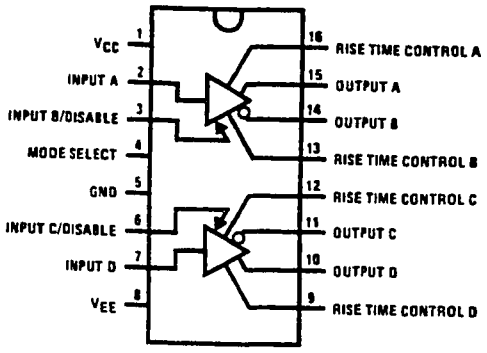
With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE control for individual outputs
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- Individual rise mode time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422 35 mW/driver typ
  - RS-423 26 mW/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Pin compatible with AM26LS30

Connection Diagram

With Mode Select LOW
(RS-422 Connection)



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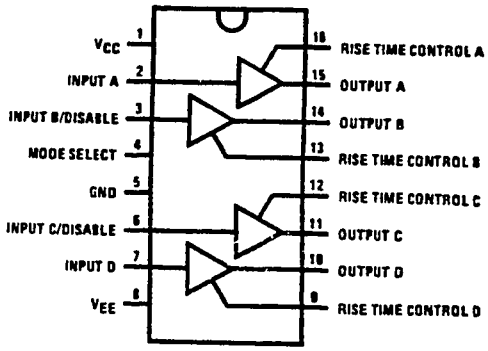
Top View

With Mode Select HIGH
(RS-423 Connection)



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Top View

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J, DS3691M or DS3691N
See NS Package Number J16A, M16A or N16A

Figure C-6: Tri-state line driver (National Semiconductor ref. 25).

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to + 150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$			V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage $V_{A,B}$	R_L = 100Ω, V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$			V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE}$ = 2.4V		±10			V
I_{XA}	Output Leakage Current Power OFF	V_{CC} = 0V	V_{CMR} = 10V			100	μA
I_{XB}			V_{CMR} = −10V			−100	μA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max	V_{CMR} ≤ 10V			100	μA
			V_{CMR} ≥ −10V			−100	μA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA

Figure C-6 (continued): Tri-state line driver (National Semiconductor).

AC Electrical Characteristics $T_A = 25°C$ (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, $V_{CC} = 5V$, MODE SELECT = 0.8V						
t_r	Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_f	Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF *(Figure 4)*		250	350	ns
t_{PZH}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF *(Figure 4)*		180	300	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF *(Figure 4)*		180	300	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF *(Figure 4)*		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\|V_{CC}\| = \|V_{EE}\|$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
V_O	Output Voltage	$R_L = \infty$, (Note 6) $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	4.0	4.4	6.0	V
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	V
V_T	Output Voltage	$R_L = 450\Omega$ $V_{CC} \geq 4.75V$	$V_{IN} = 2.4V$	3.6	4.1		V
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\| = 4.75V$, $R_L = 450\Omega$			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = 6V$		2	100	μA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = -6V$		−2	−100	μA
I_S^+	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
I_S^-	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characterisbcs" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

Figure C-6 (continued): Tri-state line driver (National Semiconductor).

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} = −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		µs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF *(Figure 3)*		0.06		µs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns

AC Test Circuits and Switching Time Waveforms

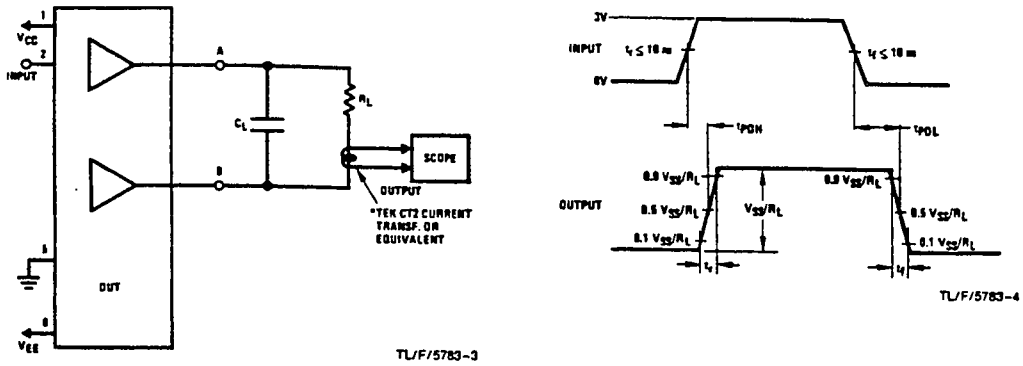


FIGURE 1. Differential Connection

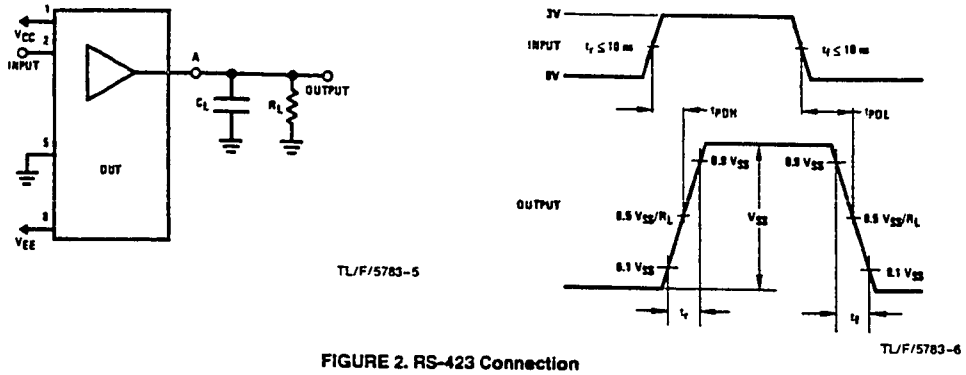


FIGURE 2. RS-423 Connection

Figure C-6 (continued): Tri-state line driver (National Semiconductor).

AC Test Circuits and Switching Time Waveforms (Continued)

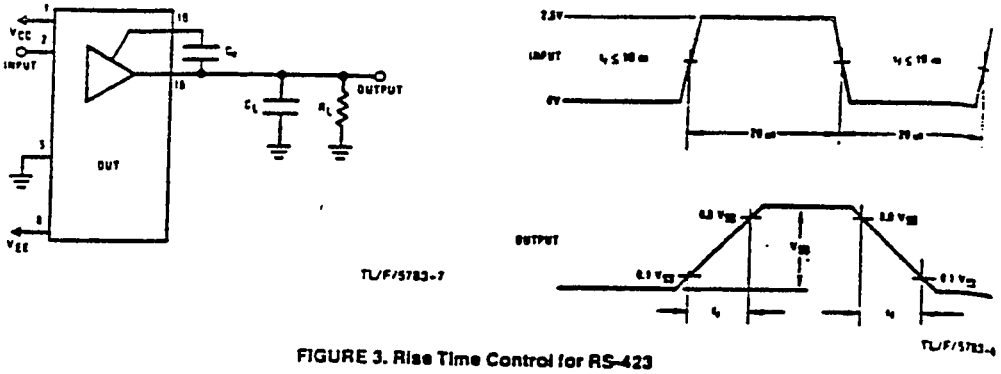


FIGURE 3. Rise Time Control for RS-423

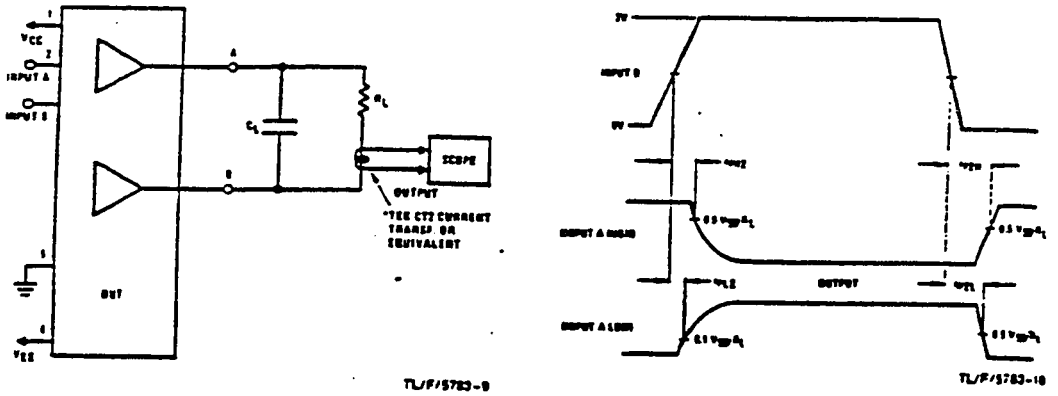


FIGURE 4. TRI-STATE Delays

Switching Waveforms

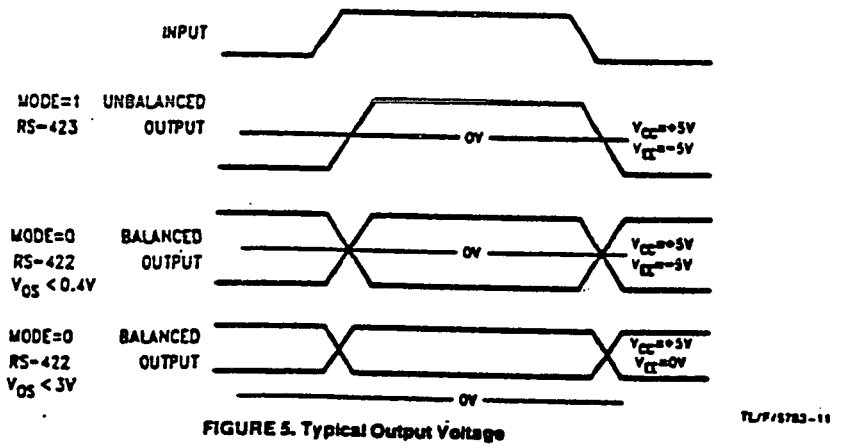
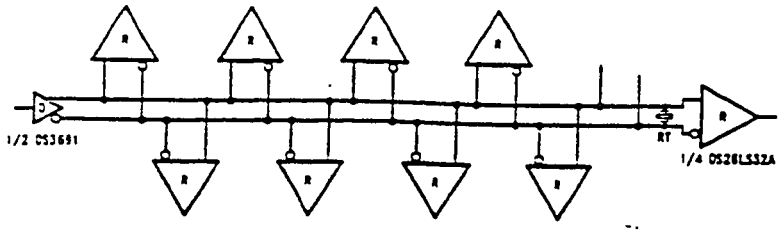


FIGURE 5. Typical Output Voltage

Figure C-6 (continued): Tri-state line driver (National Semiconductor).

Typical Application Information

Fully Loaded RS-422 Interface



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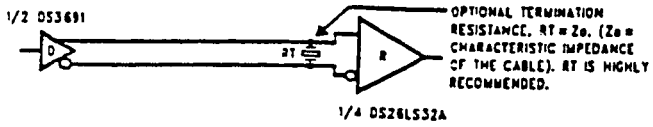
RS-422 Point to Point Application



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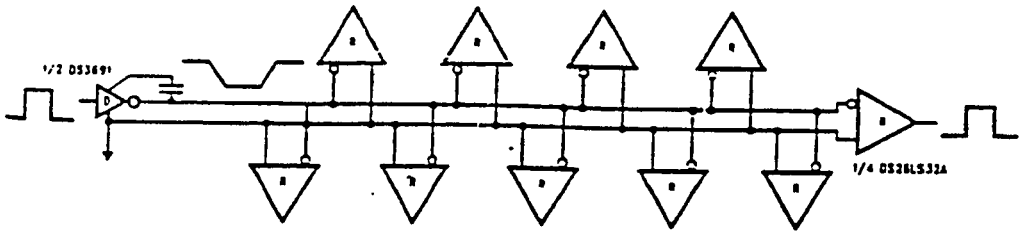
Fully Loaded RS-423 Interface



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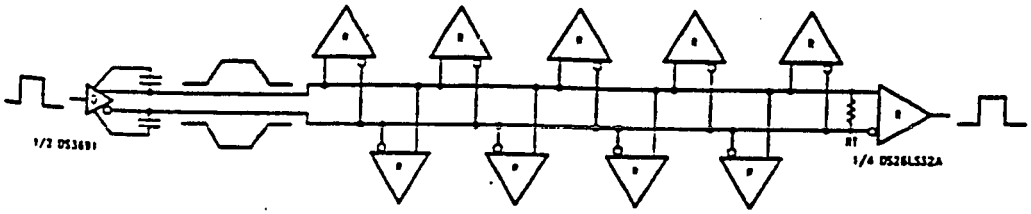
Differential Application with Rise Time Control



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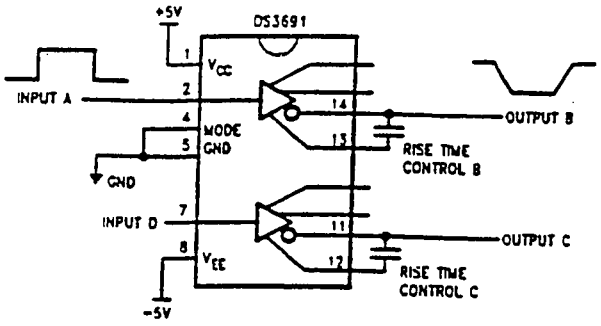
*Note: Controlled edge allows longer stub lengths. Multiple Drivers are NOT allowed

Figure C-6 (continued): Tri-state line driver (National Semiconductor).

Typical Application Information (Continued)

Dual RS-423 Inverting Driver



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Typical Rise Time Control Characteristics (RS-423 Mode)

Rise Time vs External Capacitor

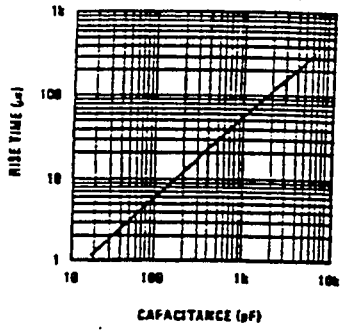

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Figure C-6 (concluded): Tri-state line driver (National Semiconductor).

HEWLETT PACKARD

Versatile Link
The Versatile Fiber Optic Connection

Technical Data

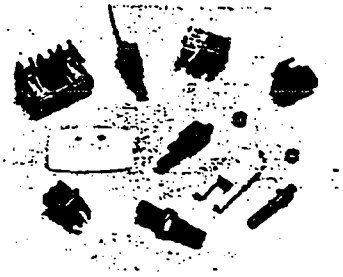
HFBR-0501 Series

Features

- **Low Cost Fiber Optic Components**
- **Guaranteed Link Performance over Temperature**
  Enhanced High Speed Links 2-50 MBd
  High Speed Links: dc to 5 MBd
  Extended Distance Links: up to 111 meters
  Low Current Link: 6 mA Peak Supply Current
  Low Cost Standard Link: dc to 1 MBd
  Photo-interrupter Link
- **Compact, Low Profile Packages**
  Horizontal and Vertical Mounting
  Interlocking Feature
  Flame Retardant
- **Easy to Use Receivers**
  TTL, CMOS Compatible Output Level
  High Noise Immunity
- **Easy Connectoring**
  Simplex, Duplex, and Latching Connectors
  Flame Retardant Material
- **Low Attenuation 1 mm Plastic Cable**
  Simplex and Zip Cord Style Duplex
  Extra Low Loss Simplex and Duplex
  UL VW-1 Flame Retardancy Conformance
- **No Optical Design Required**
- **Auto-Insertable and Wave Solderable**
- **Demonstrated Reliability at 40°C Exceeds 2 Million Hours MTBF**

Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0501 series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The Link design is simplified by the logic compatible receivers and



complete specifications for each component. No optical design is necessary. The key optical and electrical parameters of links configured with the HFBR-0501 family are fully guaranteed from 0° to 70°C. A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Figure C-7: Fiber optic link system (Hewlett Packard ref.26).

Versatile Link Applications

- Reduction of lightning/ voltage transient susceptibility
- Motor controller triggering
- Data communications and Local Area Networks
- Electromagnetic Compatibility (EMC) for regulated systems: FCC, VDE, CSA, etc.
- Tempest-secure data processing equipment
- Isolation in test and measurement instruments
- Error free signaling for industrial and manufacturing equipment
- Power supply control
- Communication and isolation in medical instruments
- Noise immune communication in audio and video equipment
- Remote photo interrupter for office and industrial equipment
- Robotics communication
- PC to peripheral links
- Intra-system links; board-to-board, rack-to-rack
- Digitized video
- Medical instruments

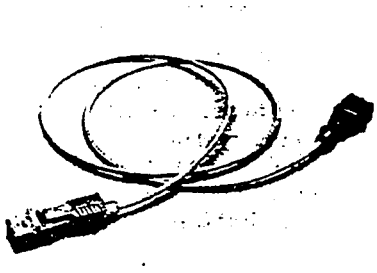
Link Selection Guide

Versatile Link		Guaranteed Minimum Link Length (Meters)				Typical Link Length (Meters)	
		0°C-70°C		25°C		25°C	
		Standard Cable	Extra Low Loss Cable	Standard Cable	Extra Low Loss Cable	Standard Cable	Extra Low Loss Cable
50 MBd Link	50 MBd	15	17	–	–	59	65
High Performance	5 MBd	19	22	27	32	48	53
High Performance	1 MBd	39	45	47	56	70	78
Low Current Link	40 kBd	13	15	–	–	41	45
Extended Distance Link	40 kBd	94	111	103	121	138	154
Standard	1 MBd	8	10	17	20	43	48
Photo Interrupter	500 kHz	NA	NA	NA	NA	NA	NA
Evaluation Kit	1 MBd (Standard)	Contents: Horizontal transmitter, horizontal receiver packages; 5 meters of simplex cable with simplex and simplex latching connectors installed; individual connectors: simplex, duplex, simplex latching, bulkhead adapter, polisihng tool, abrasive paper, literature.					

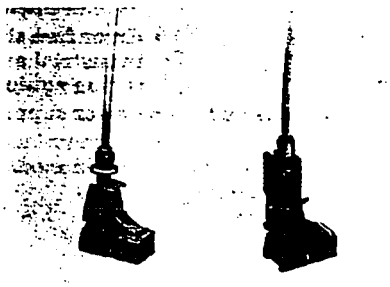
Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Versatile Link Product Family

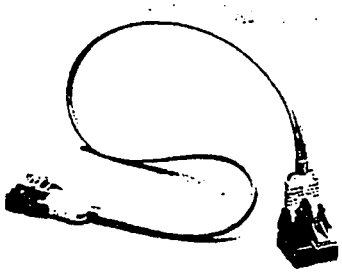
50 MBd, 5 MBd, 1 MBd and 40 kBd Fiber Optic Links



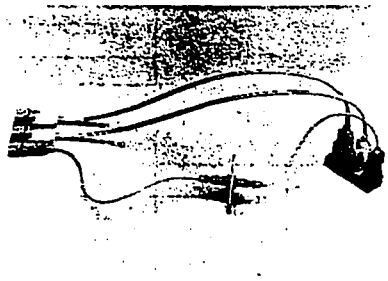
Simplex Link–Horizontal Packages



Simplex Link–Vertical Packages



Duplex Link–Combination of Horizontal & Vertical Packages



N-Plex Link–Combinations

Versatile Link Product Description

Mechanical: The compact Versatile Link package is made of a flame retardant material (UL V-0) in a standard, eight pin dual-in-line package (DIP) with 7.6 millimeter (0.3 inch) pin spacing. Vertical and horizontal mountable parts are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Electrical: Transmitters incorporate a 660 nanometer light emitting diode (LED). Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1/2/4 receivers. Transmitter and receiver are compatible with standard TTL circuitry. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Optical: Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all component interface losses. Therefore, the need of optical calculations for common link applications is eliminated.

Optical power budget is graphically displayed to facilitate electrical design for customized links.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Designing with Versatile Link

When designing with Versatile Link the following topics should be considered:

Distance and Data Rate

Distances and data rates guaranteed with Versatile Link depend upon the Versatile Link transmitter/receiver pair chosen.

Typically a data rate requirement is first specified. This determines the choice of the 50 MBd, 5 MBd, 1 MBd, or 40 kBd Versatile Link components. Distances guaranteed with Versatile Link then depend upon choice of cable, specific drive condition and circuit configuration. Extended distance operation is possible with pulsed operation of the LED (see Figure 2a, 2b, 2c, 2d, 2e, and 2f dotted lines.)

Drive circuits are described in the Link Design sections. Cable is discussed in the Plastic Cable section. Pulsed operation of the LED at larger current will result in increased pulse width distortion of the receiver output signal.

Versatile Link can also be used as a photo interrupter at frequencies up to 500 KHz.

Package Orientation

As shown in the photograph Versatile Link is available in vertical and horizontal packages. Performance and pinouts for the two packages are identical. To provide additional attachment support for the Vertical Versatile Link housing, the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion when making connections. The HFBR-15X1/2/4/6 transmitters are gray and the HFBR-25X1/2/3/4/6 receivers are blue. The HFBR-15X3 transmitter is black.

All of the above transmitter and receivers are also available in black versions for special applications. These black components combined with black fiber optic cable form a "black link" which has superior immunity to external light. The black link is appropriate where improved housing opacity is required due to very bright ambient light or bright flashes of light. Black link components are otherwise identical to blue and gray components.

Connector Style

As shown, Versatile Link can be used with snap-in connectors: simplex, simplex latching, duplex, and duplex latching.

The simplex connector is intended for applications requiring simple, stable connection capability with a moderate retention force. The simplex latching connector provides similar convenience with a larger retention force. Connector/cable retention force can be improved by using an RTV adhesive within the connector. A suggested adhesive is GE Company RTV-128 or Dow Corning 3154.

The duplex connector connects a cable containing two fibers to two similar Versatile Link components. A lockout feature ensures the connection can be made in only one orientation. The duplex connector is intended for Versatile Link components interlocked together as discussed in the next section.

Stacking

Versatile Link components can be stacked or interlocked together to minimize use of printed circuit board space and provide efficient, dual connections with the duplex connector. Up to eight identical package styles can be interlocked and inserted by hand into a printed circuit board without difficulty. However, auto-insertion of stacked units becomes limited when more than two packages are interlocked together.

Plastic Cable

Two 1 mm plastic cable versions are available: simplex (single channel) and marked duplex (dual channel). Each version of the low optical loss cable complies with the UL VW-1 flame retardancy specification. Two grades of plastic cable are available: standard attenuation and extra low-loss attenuation. Extra low-loss cable is recommended for applications requiring longer distance needs, as reflected in the Link Selection Guide. Flexible cable construction allows simple cable installation techniques. Cables are discussed in detail in the Plastic Cable section.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Accessories

A variety of accessories are available. The bulkhead feed-through adapter discussed in the Mechanical Dimensions section is designed to mate two simplex snap-in connectors to act as either a splice or panel feedthrough for a panel thickness <4.1 mm (0.16 inch).

Several accessories are offered to help with proper fiber/connector polishing. These are shown in the Mechanical Dimensions section.

Manufacturing with Versatile Link

Non-stacked Versatile Link parts require no special handling during assembly of units onto printed circuit boards. Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, an optical port plug is recommended to be used to prevent contamination of the port. Water soluble fluxes, not rosin based fluxes, are recommended for use with Versatile Link components.

Refer to the Connectoring Section for details of connectors and cable connectoring.

Versatile Link Performance

50 MBd Link Performance

The HFBR-15X6 transmitter is a 660 nm LED in a low cost plastic housing designed to efficiently couple power into 1 mm diameter plastic optical fiber. With the recommended drive circuit, the LED operates at speeds from 2-50 MBd. The HFBR-25X6 is a high bandwidth analog receiver with a PIN photo diode and internal transimpedance amplifier. The transmitter and receiver interface to plastic optical fiber, which is easily terminated with the HP Versatile Link family connectors. These components can be used for high speed data links without the problems common to copper wire solutions at a competitive cost.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

5 MBd, 1 MBd, and 40 kBd Link Performance

The 5 Megabaud (MBd) Versatile Link is guaranteed to perform from dc to 5 Mb/s (megabits per second, NRZ). Distances up to 22 meters are guaranteed when the transmitter is driven with a current of 60 milliamperes. This represents worst case performance throughout the temperature range of 0 to 70 degrees centigrade. With the required drive circuit of Figure lb and at 60 milliamp drive current, the High Performance 1 Megabaud Versatile Link has guaranteed performance over 0° to 70°C from dc to 1 Mb/s (NRZ) up to 45 meters.

The low current link requires only 6 mA peak supply current for the transmitter and receiver combined to achieve a 15 meter link. Extended distances up to 111 meters can be achieved at a maximum transmitter drive current of 60 mA peak. The 40 kBd Versatile Link is guaranteed to perform from dc to 40 kb/s (NRZ) over 0° - to 70°C up to the distances just described.

Receivers are compatible with LSTTL, TTL, CMOS logic levels and offer a choice of an internal pull-up resistor or an open collector output. Horizontal or vertical packages provide identical performance and are compatible with simplex, simplex latching, duplex, and duplex latching connectors. Refer to the Connector Section and the Cable Section for further information about these products. A list of specific part numbers is found below and in the Link Selection Guide.

5 MBd, 1 MBd, and 40 kBd Link Guide

Versatile Link		Unit	Horizontal Package	Vertical Package	Cable Link Length (0°C-70°C)	
					Standard Cable	Extra Low Loss Cable
High Performance	5 MBd	Tx	HFBR-1521	HFBR-1531	19 meters	22 meters
		Rx	HFBR-2521	HFBR-2531		
High Performance	1 MBd	Tx	HFBR-1522	HFBR-1532	39 meters	45 meters
		Rx	HFBR-2522	HFBR-2532		
Low Current/ Extended Distance	40 kBd	Tx	HFBR-1523	HFBR-1533	13 meters/ 94 meters	15 meters/ 111 meters
		Rx	HFBR-2523	HFBR-2533		
Standard	1 MBd	Tx	HFBR-1524	HFBR-1534	8 meters	10 meters
		Rx	HFBR-2524	HFBR-2534		

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Ref.
Ambient Temperature		T_A	0	70	°C	
Transmitter Peak Forward Current		$I_{F\,PK}$	10	750	mA	Note 1, 8
Average Forward Current		$I_{F\,AV}$		60	mA	
Receiver Supply Voltage	HFBR-25X3	V_{CC}	4.50	5.50	V	Note 2
	HFBR-25X1/25X2/25X4		4.75	5.25		
Output Voltage	HFBR-25X3	V_O		V_{CC}	V	
	HFBR-25X1/25X2/25X4			18		
Fanout (TTL)	HFBR-25X3	N		1		
	HFBR-25X1/25X2/25X4			5		

System Performance Under recommended operating conditions unless otherwise specified.

Link	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
High Performance 5 MBd	Data Rate		dc		5	MBd	BER ≤ 10^{-9}, PRBS: $2^7 - 1$	
	Link Distance with Standard Cable	ℓ	19			m	I_{Fdc} = 60 mA	Fig. 2a Note 7
			27	48		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable	ℓ	22			m	I_{Fdc} = 60 mA	Fig. 2b Note 7
			32	53		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		80	140	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre -21.6 ≤ P_R ≤ -9.5 dBm	Fig. 3, 5 Notes 3, 6
		t_{PHL}		50	140	ns		
	Pulse Width Distortion	t_D		30		ns	P_R = -15 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Note 4
High Performance 1 MBd	Data Rate		dc		1	MBd	BER ≤ 10^{-9}, PRBS: $2^7 - 1$	
	Link Distance with Standard Cable	ℓ	39			m	I_{Fdc} = 60 mA	Fig. 2a Notes 1, 7, 8
			47	70		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable	ℓ	45			m	I_{Fdc} = 60 mA	Fig. 2b Notes 1, 7, 8
			56	78		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -24 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

System Performance Under recommended operating conditions unless otherwise specified, contd.

Link	Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Low Current/ Extended Distance 40 kBd	Data Rate		dc		40	kBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	13	41		m	I_{Fdc} = 2 mA	Fig. 2c Note 7
			94	138		m	I_{Fdc} = 60 mA	
	Link Distance with Extra Low Loss Cable	ℓ	15	45		m	I_{Fdc} = 2 mA	Fig. 2d Note 7
			111	154		m	I_{Fdc} = 60 mA	
	Propagation Delay	t_{PLH}		4		µs	R_L = 3.3 kΩ, C_L = 30 pF ℓ = 1 metre P_R = -25 dBm	Fig. 3, 7 Note 3
		t_{PHL}		2.5		µs		
	Pulse Width Distortion	t_D			7.0	µs	-39 ≤ P_R ≤ -14 dBm R_L = 3.3 kΩ, C_L = 30 pF	Fig. 3, 6 Note 4
Standard 1 MBd	Data Rate	ℓ	dc		1	MBd	BER ≤ 10^{-9}, PRBS: 2^7 - 1	
	Link Distance with Standard Cable	ℓ	8			m	I_{Fdc} = 60 mA	Fig. 2e Notes 1, 7, 8
			17	43		m	I_{Fdc} = 60 mA, 25°C	
	Link Distance with Extra Low Loss Cable		10			m	I_{Fdc} = 60 mA	Fig. 2f Notes 1, 7, 8
			19	48		m	I_{Fdc} = 60 mA, 25°C	
	Propagation Delay	t_{PLH}		180	250	ns	R_L = 560 Ω, C_L = 30 pF ℓ = 0.5 metre P_R = -20 dBm	Fig. 3, 5 Notes 3, 8
		t_{PHL}		100	140	ns		
	Pulse Width Distortion	t_D		80		ns	P_R = -20 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 3, 4 Notes 4, 8

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{FDC} ≤ 80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   I_{FPK} ≤ 160 mA: Pulse width ≤ 1 ms
   I_{FPK} ≥ 160 mA: Pulse width ≤ 1 µs, period ≥ 20 µS.
2. It is essential that a bypass capacitor, 0.1 µF ceramic, be connected from pin 2 to pin 3 of the HFBR-25X1/25X2/25X4 receivers and from pin 2 to pin 4 of the HFBR-25X3 receiver. Total lead length between both ends of the capacitor and the supply pins should not exceed 20 mm.
3. The propagation delay for one metre of cable is typically 5 ns.
4. $t_D = t_{PLH} - t_{PHL}$.
5. Typical data is at 25°C, V_{CC} = 5 V.
6. Typical propagation delay is measured at P_R = -15 dBm.
7. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
8. Pulsed LED operation at I_{FPK} > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
9. Pins 5 and 8 of both the transmitter and receiver are for mounting and retaining purposes only. Do not electrically connect pin 5 and/or pin 8.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

5 MBd, 1 MBd, and 40 kBd Link Design Considerations

Simple interface circuits for use with the 5 MBd, 1 MBd and 40 kBd Versatile Links are shown in Figure 1. The value of the transmitter drive current depends upon the desired link distance. This is shown in Figures 2a through 2f. After selecting a value of transmitter drive current, I_F, the value of R1 can be determined with the aid of Figures 1a, 1b, and 1d. Note that the 5 MBd and 40 kBd Versatile Links can have an overdrive and underdrive limit for the chosen value of I_F while the 1 MBd Versatile Link has only an underdrive limit. Dotted lines in Figures 2a through 2f represent pulsed operation for extended link distance requirements. For the HFBR-1522/1532/1524/1534 interface circuit, the R1C1 time constant must be > 75 ns. Conditions described in Note 1 must be met for pulse operation. Refer to Note 8 for performance comments when pulse operation is used.

All specifications are guard-banded for worst case conditions between 0 to 70 degrees centigrade. All tolerances and variations (including end-of-line transmitter power, receiver sensitivity, coupling variances connector and cable variations) are taken into account.

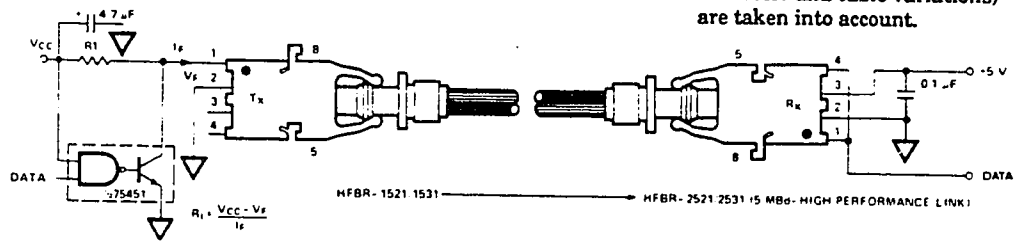


Figure 1a. Typical Interface Circuit for the HFBR-1521/1531, the 5 MBd Versatile Link (dc to 5 MBd).

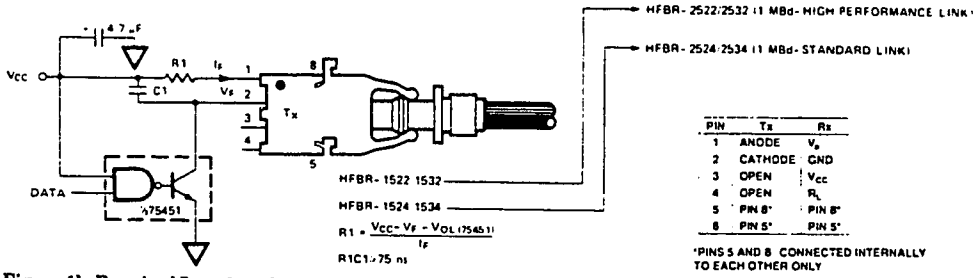


Figure 1b. Required Interface Circuit for the HFBR-1522/1532/1524/1534, the 1 MBd Versatile Link (dc to 1 MBd).

PIN	Tx	Rx
1	ANODE	V_o
2	CATHODE	GND
3	OPEN	V_{CC}
4	OPEN	R_L
5	PIN 8*	PIN 8*
8	PIN 5*	PIN 5*

*PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY

Figure 1c. Electrical Pin Assignments for 5 MBd and 1 MBd Transmitters and Receivers.

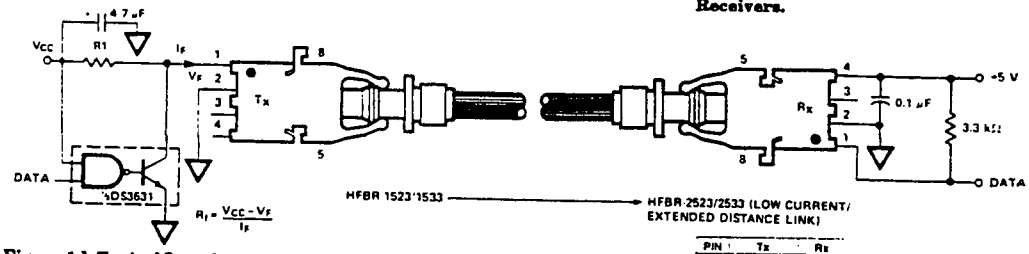


Figure 1d. Typical Interface Circuit for the HFBR-1523/1533, the 40 kBd Versatile Link (dc to 40 kBd).

PIN	Tx	Rx
1	ANODE	V_o
2	CATHODE	GND
3	OPEN	OPEN
4	OPEN	V_{CC}
5	PIN 8*	PIN 8*
8	PIN 5*	PIN 5*

*PINS 5 AND 8 CONNECTED INTERNALLY TO EACH OTHER ONLY

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

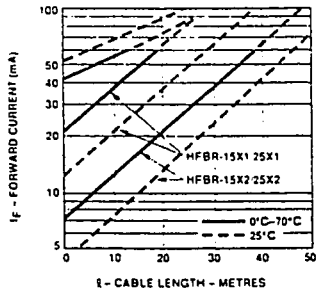


Figure 2a. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Standard Cable.

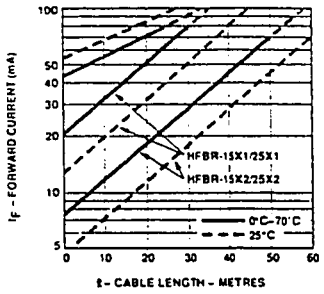


Figure 2b. Guaranteed System Performance for the HFBR-15X1/25X1 and HFBR-15X2/25X2 Links with Extra Low Loss Cable.

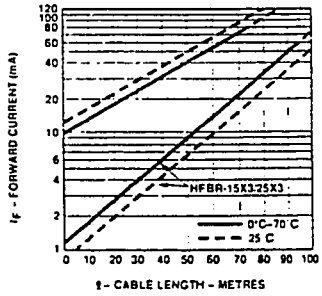


Figure 2c. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Standard Cable.

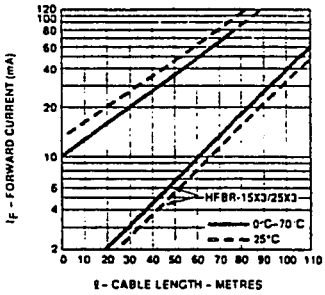


Figure 2d. Guaranteed System Performance for the HFBR-15X3/25X3 Link with Extra Low Loss Cable.

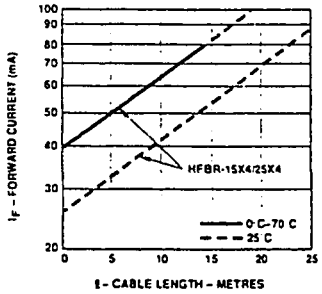


Figure 2e. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Standard Cable.

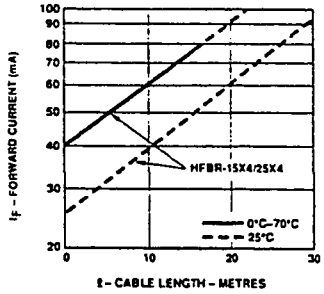


Figure 2f. Guaranteed System Performance for the HFBR-15X4/25X4 Link with Extra Low Loss Cable.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

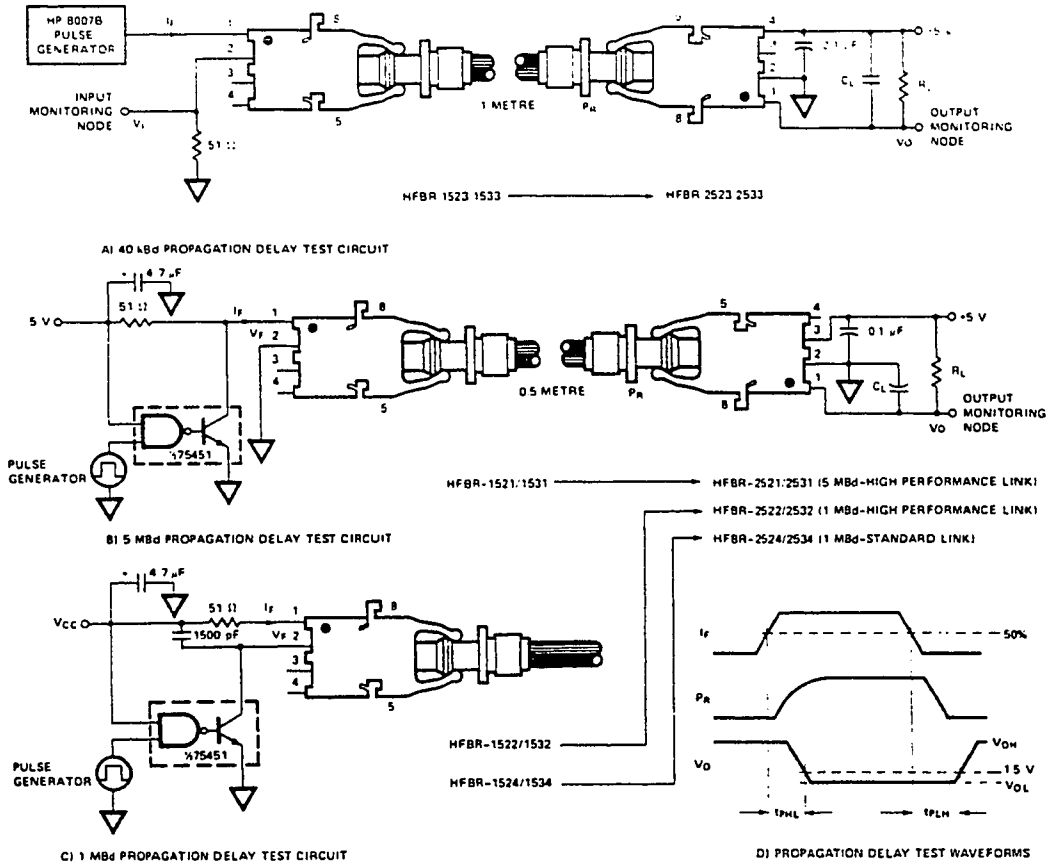


Figure 3. Propagation Delay Test Circuits and Waveforms: a) 40 kBd, b) 5 MBd, c) 1 MBd, d) Test Waveforms.

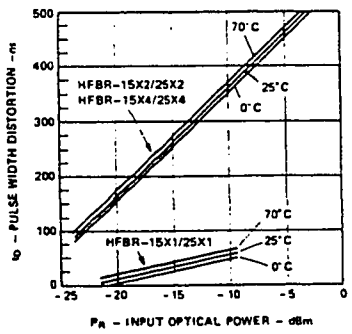


Figure 4. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Pulse Width Distortion vs. Optical Power.

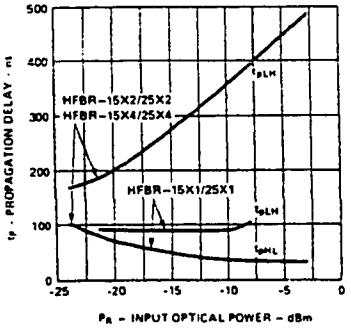


Figure 5. Typical HFBR-15X1/25X1, HFBR-15X2/25X2 and HFBR-15X4/25X4 Link Propagation Delay vs. Optical Power.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

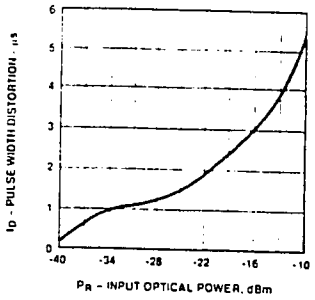


Figure 6. Typical HFBR-15X3/-25X3 Link Pulse Width Distortion vs. Optical Power.

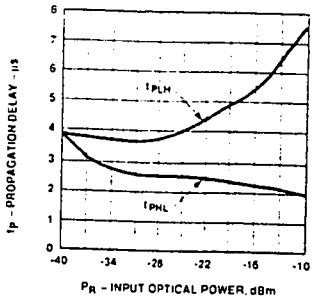


Figure 7. Typical HFBR-15X3/-25X3 Link Propagation Delay vs. Optical Power.

Photo-interrupter Link Performance

20 kHz (40 kBd) Link, 500 kHz (1 MBd) Link

Versatile Link may be used as a photo-interrupter in optical switches, shaft position sensors, velocity sensors, position sensors, and other similar applications. This link is particularly useful where high voltage, electrical noise, or explosive environments prohibit the use of electromechanical or optoelectronic sensors. The 20 kHz (40 kBd) transmitter/receiver pair has an optical power budget of 25 dB. The 500 kHz (1 MBd) transmitter/receiver pair has an optical power budget of 10 dB. Total system losses (cable attenuation, air gap loss, etc.) must not exceed the link optical power budget.

Recommended Operating Conditions

Recommended operating conditions are identical to those of the Low Current/Extended Distance and High Performance 1 MBd links. Refer to page 15.

System Performance

These specifications apply when using Standard and Extra-Low Loss cable and, unless otherwise specified, under recommended operating conditions. Refer to the appropriate link data on pages 5-17 and 5-18 for additional design information.

Parameter	Min.	Typ.[1]	Max.	Units	Conditions	Ref.
HFBR-15X3/25X3						
Max. Count Frequency	dc		20	kHz		
Optical Power Budget	25.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	27.8	34		dB	I_{Fdc} = 60 mA, 25°C	
HFBR-15X2/25X2						
Max. Count Frequency	dc		500	kHz		
Optical Power Budget	10.4			dB	I_{Fdc} = 60 mA, 0-70°C	Note 2
	12.8	15.6		dB	I_{Fdc} = 60 mA, 25°C	

1. Typical data is at T_A = 25°C. V_{CC} = 5 V.
2. Optical Power Budget = P_T min. = P_R (L) min. Refer to the Link Design section for additional design information.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Photo-interrupter Link Design Considerations

The fiber optic Transmitter/ Receiver pair is intended for applications where the photo interrupter must be physically separated from the optoelectronic emitter and detector This separation would be useful where high voltage, electrical noise or explosive environments prohibit the use of electronic devices. To ensure reliable long term operation, link design for this application should operate with an ample optical power margin $\alpha_M \geq 3$ dB, since the exposed fiber ends are subject to environmental contamination that will increase the optical attenuation of the slot with time. A graph of air gap separation versus attenuation for clean fiber ends with minimum radial error ≤ 0.127 mm (0.005 inches) and angular error (≤3.0°) is provided In Figure 8.

The following equations can be used to determine the transmitter output power, P_T, for both the overdrive and underdrive cases. Overdrive is defined as a condition where excessive optical power is delivered to the receiver. The first equation calculates, for a predetermined link length and slot attenuation. The maximum P_T in order not to overdrive the receiver The second equation defines the minimum P_T allowed for link operation to prevent underdrive condition from occurring, where α_o is the fiber attenuation.

$$P_T (MAX) - P_R (MAX) \leq \alpha_{o\ MIN}\, \ell + \alpha_{SLOT} \quad \text{Eq. 1}$$

$$P_T (MIN) - P_{RL} (MIN) \geq \alpha_{o\ MAX}\, \ell + \alpha_{SLOT} + \alpha_M \quad \text{Eq. 2}$$

Once P_T (MIN) has been determined in the second equation for a specific link length (l), slot attenuation (α_{SLOT}) and margin (α_M). Figure 9 can then be used to find I_F.

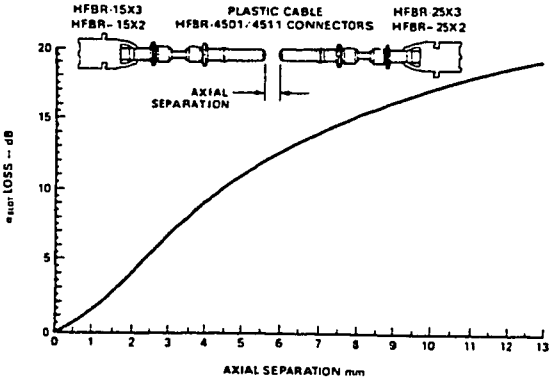


Figure 8. Typical Loss vs. Axial Separation.

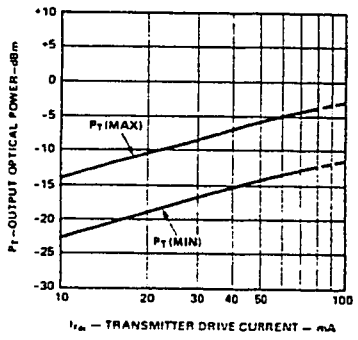


Figure 9. Typical HFBR-15X3/15X2 Optical Power vs. Transmitter I_F (0-70°C).

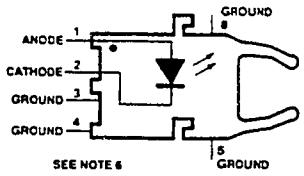
Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Versatile Link Transmitters and Receivers

50 MBd Link Transmitters

HFBR-1526/-1536 (50 MBd)

The HFBR-15X6 transmitters incorporate a 660 nanometre LED in a horizontal (HFBR-1526) or vertical (HFBR-1536) gray housing. The HFBR-15X6 transmitters are suitable for use with current peaking to decrease the response times, and can be used with HFBR-25X6 receivers in data links operating at signal rates from 2 to 50 megabaud over 1 mm diameter plastic optical fiber. Refer to Application Note 1045 for details of recommended interface circuits.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature	T_S	-40	75	°C	
Operating Temperature	T_A	0	70	°C	
Lead Soldering Temperature			260	°C	Note 1
Cycle Time			3	s	
Forward Input Current Peak	I_{FPK}		500	mA	15 % duty cycle ≥ 1 KHz
Forward Input Current Average	I_{Favg}		80	mA	
Reverse Input Voltage	V_R		5	V	

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Electrical/Optical Characteristics 0 to 70°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.[2]	Max.	Unit	Condition	Ref.
Peak Output Optical Power	P_T	-12.0	-9.6	-7.8	dBm	I_{Fdc} = 60 mA, 25°C	Note 3
		-13.6		-6.9	dBm	I_{Fdc} = 60 mA, 0-70°C	
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.036		dB/°C	I_{Fdc} = 60 mA	
Peak Emission Wavelength	λ_{PK}	655	660	670	nm	25°C	
		645		680	nm	0-70°C	
Spectral Width	FWHM			30	nm	Full Width, Half Maximum	
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.37		mV/°C	I_{Fdc} = 60 mA	
Thermal Resistance, Junction to Case	θ_{jc}		140		°C/W		Note 4
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = -10 μA, 25°C	
Diode Capacitance	C_O		100		pF	V_F = 0 f = 1 MHz	
Unpeaked Optical Rise Time, 10%-90%	t_r		45		ns	I_{Fdc} = 60 mA f = 100 kHz	Figure 1, Note 5
Unpeaked Optical Fall Time, 90%-10%	t_f		20		ns	I_{Fdc} = 60 mA f = 100 kHz	Figure 1, Note 5

Notes:

1. 1.6 mm below seating plane.
2. Typical data is at 25°C.
3. Optical power measured at the end of 0.5 metres of 1 mm diameter plastic optical fiber with large area detector.
4. Typical value measured from junction to PC board solder joint for horizontal mount package, HFBR-1526. θ_{jc} is approximately 30°C/W higher for vertical mount package, HFBR-1536.
5. Optical rise and fall times can be reduced with the appropriate driver circuit; refer to Application Note 1045.
6. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected; pins 3 and 4 are electrically unconnected. It is recommended that pins 3, 4, 5, and 8 all be connected to ground to reduce coupling of electrical noise.
7. Refer to VERSATILE LINK HFBR-0501 Series Technical Data Sheet, for cable connector options.
8. The LED current peaking necessary for high frequency circuit design contributes to electromagnetic interference (EMI). Care must be taken in circuit board layout to minimize emissions for compliance with governmental EMI emissions regulations. Refer to Application Note 1045 for design guidelines.

WARNING: When viewed under some conditions, the optical port may expose the eye beyond the Maximum Permissible Exposure recommended in ANSI Z136.1, 1981. Under most viewing conditions there is no eye hazard.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

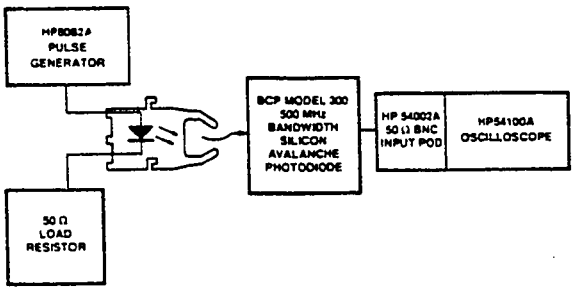


Figure 1. Test Circuit for Measuring Rise and Fall Times.

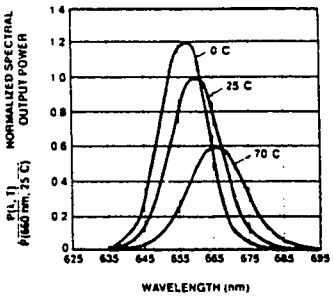


Figure 2. Typical Transmitter Spectra Normalized to the Peak at 25°C.

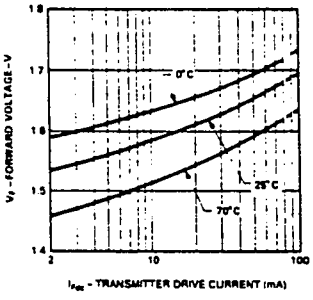


Figure 3. Typical Forward Voltage vs. Drive Current for HFBR-1526/ 1536 Transmitters.

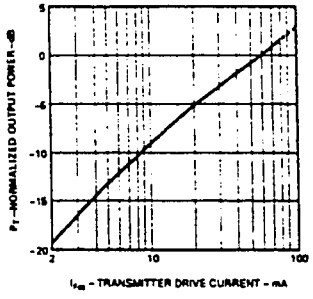
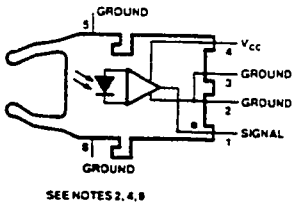


Figure 4. Normalized HFBR-1526/ 1536 Transmitter Typical Output Optical Power vs. Drive Current.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

50 MBd Link Receivers

HFBR-2526/-2536 (50 MBd)
The HFBR-25X6 receivers contain a PIN photodiode and transimpedance pre-amplifier circuit in a horizontal (HFBR-2526) or vertical (HFBR-2536) blue housing, and are designed to interface to 1 mm diameter plastic optical fiber. The receivers convert a received optical signal to an analog output voltage. Follow-on circuitry can optimize link performance for a variety of distance and data rate requirements. Electrical bandwidth greater than 65 MHz allows design of high speed data links with plastic optical fiber. Refer to Application Note 1045 for details of recommended receiver circuits.



Absolute Maximum Ratings

Parameter	Symbol	Mininum	Maximum	Unit	Reference
Storage Temperature	T_S	-40	75	°C	
Operating Temperature	T_A	0	70	°C	
Lead Soldering Temp.			260	°C	Note 1
Cycle Time			3	s	
Signal Pin Voltage	V_O	-0.5	V_{CC}	V	
Supply Voltage	V_{CC}	-0.5	6.0	V	
Output Current	I_O		25	mA	

CAUTION: The small junction sizes inherent to the design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

Electrical/Optical Characteristics 0 to 70°C; Fiber core diameter ≤ 1.0 mm, fiber N.A. ≤ 0.5. 5.25 V < V_{CC} < 4.75 V; power supply must be filtered (see Figure 1, Note 2).

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit	Condition	Reference
AC Responsivity	R_P	1.7	3.9	6.5	mV/μW	660 nm	Note 4
RMS Output Noise	V_{NO}		0.46	0.69	mV_{RMS}		Note 5
Equivalent Optical Noise Input Power, RMS	$P_{N,RMS}$		-39 0.12	-36 0.25	dBm μW		Note 5
Peak Input Optical Power	P_R			-5.8 260	dBm μW	5 ns PWD	Note 6
Output Impedance	Z_O		30		Ω	50 MHz	Note 4
DC Output Voltage	V_O	0.8	1.8	2.6	V	P_R = 0 μW	
Supply Current	I_{CC}		9	15	mA		
Electrical Bandwidth	BW_E	65	125		MHz	-3 dB electrical	
Bandwidth * Rise Time			0.41		Hz *s		
Electrical Rise Time, 10-90%	t_r		3.3	6.3	ns	P_R = -10 dBm, peak	
Electrical Fall Time, 10-90%	t_f		3.3	6.3	ns	P_R = -10 dBm, peak	
Pulse Width Distortion	PWD		0.4	1.0	ns	P_R = -10 dBm, peak	Note 7
Overshoot			4		%	P_R = -10 dBm, peak	Note 8

Notes:

1. 1.6 mm below seating plane.
2. The signal output is an emitter follower, which does not reject noise in the power supply. Consequently, the power supply must be filtered as shown in Figure 1.
3. Typical data is at 25°C and V_{CC} = +5 Vdc.
4. Pin 1 should be ac coupled to a load ≥ 510 Ω, with load capacitance less than 5 pF.
5. Measured with a 3 pole Bessel filter with a 75 MHz, -3 dB bandwidth.
6. -5.8 dBm is the maximum input optical power for which pulse width distortion is guaranteed to be less than 5 ns. Pulse width distortion is typically less than 5 ns when the input optical power is less than -3.4 dBm.
7. 10 ns pulse width, 50% duty cycle, at the 50% amplitude point of the waveform.
8. Percent overshoot is defined at: $\frac{(V_{PK} - V_{100\%})}{V_{100\%}} \times 100\%$.
9. Pins 5 and 8 are primarily for mounting and retaining purposes, but are electrically connected. It is recommended that these both be connected to ground to reduce coupling of electrical noise.
10. Refer to VERSATILE LINK HFBR-0501 Series Technical Data Sheet for cable connector options.
11. If there is no input optical power to the receiver (no transmitted signal), electrical noise can result in false triggering of the receiver. In typical applications, data encoding and error detection prevent random triggering from being interpreted as valid data. Refer to Application Note 1045 for design guidelines.

Figure C-7 (continued): Fiber optic link system (Hewlett Packard).

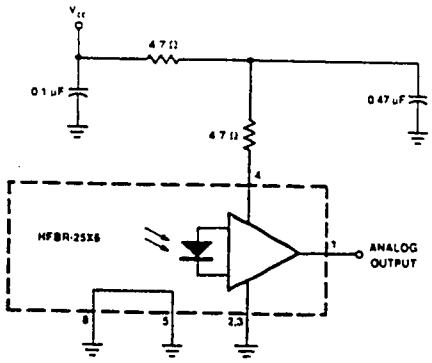


Figure 1. Recommended Power Supply Filter Circuit.

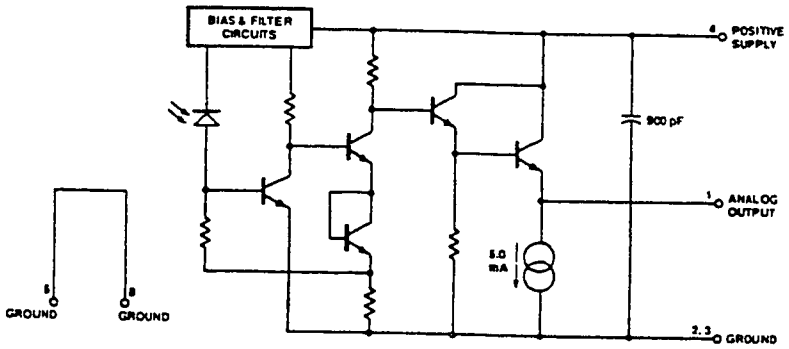


Figure 2. Simplified Receiver Schematic.

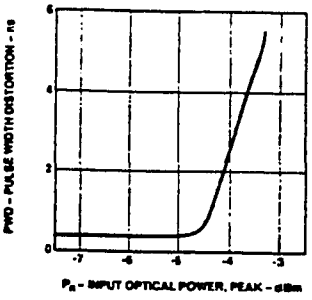


Figure 3. Typical Pulse Width Distortion vs. Peak Input Power.

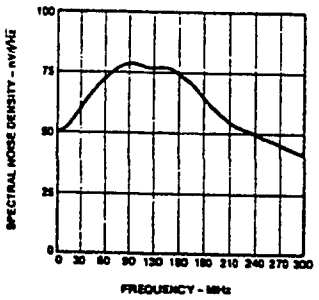


Figure 4. Typical Output Spectral Noise Density vs. Frequency.

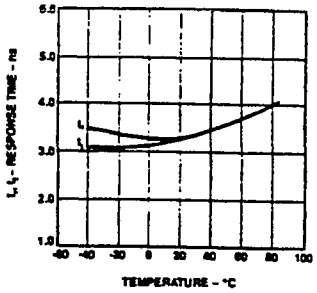


Figure 5. Typical Rise and Fall Times vs. Temperature.

Figure C-7 (concluded): Fiber optic link system (Hewlett Packard).

APPENDIX D

EXPERIMENTAL RESULTS AND WAVEFORMS

This appendix includes the results of the experimental measurements.

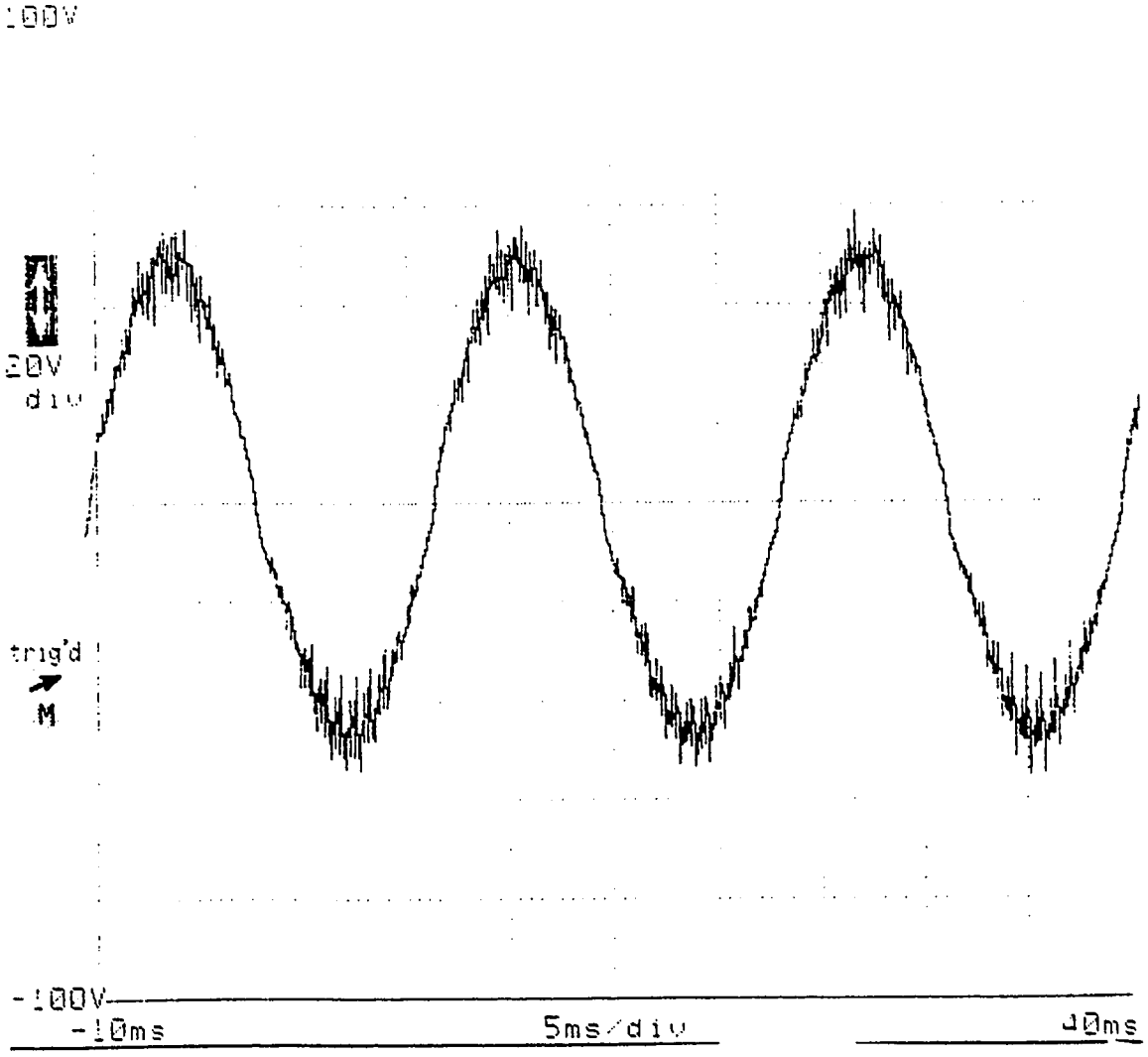


Figure D-1: Input voltage waveform.

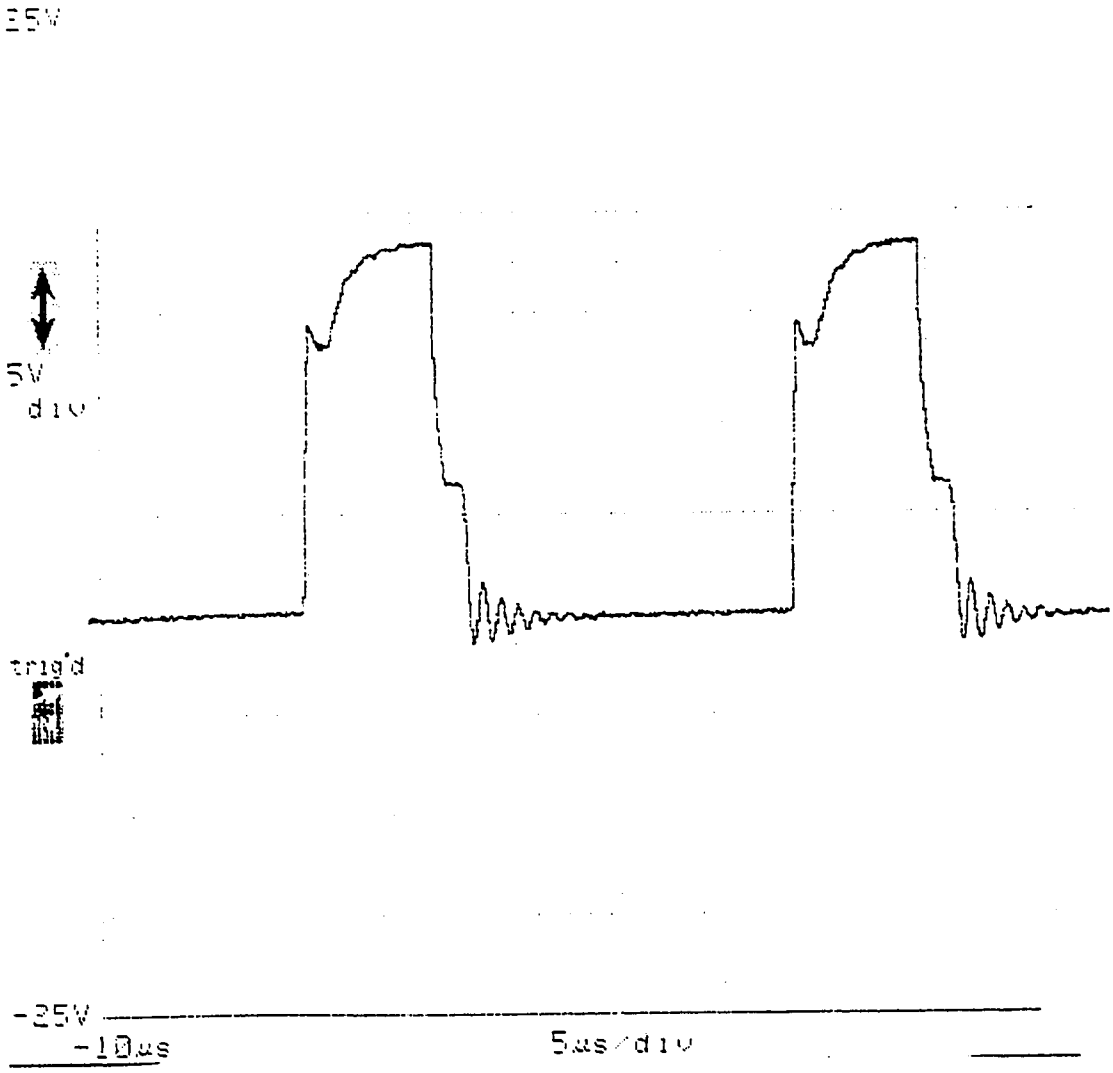


Figure D-2: Gating signal across the first transistor, T1, in the input bi-directional switch, S1, at 10 VAC at a minimum duty cycle of 0.25.

Figure D-3: Gating signal across the second transistor, T4, in the output bi-directional switch, S2, at 10 VAC at a maximum duty cycle of 0.75.

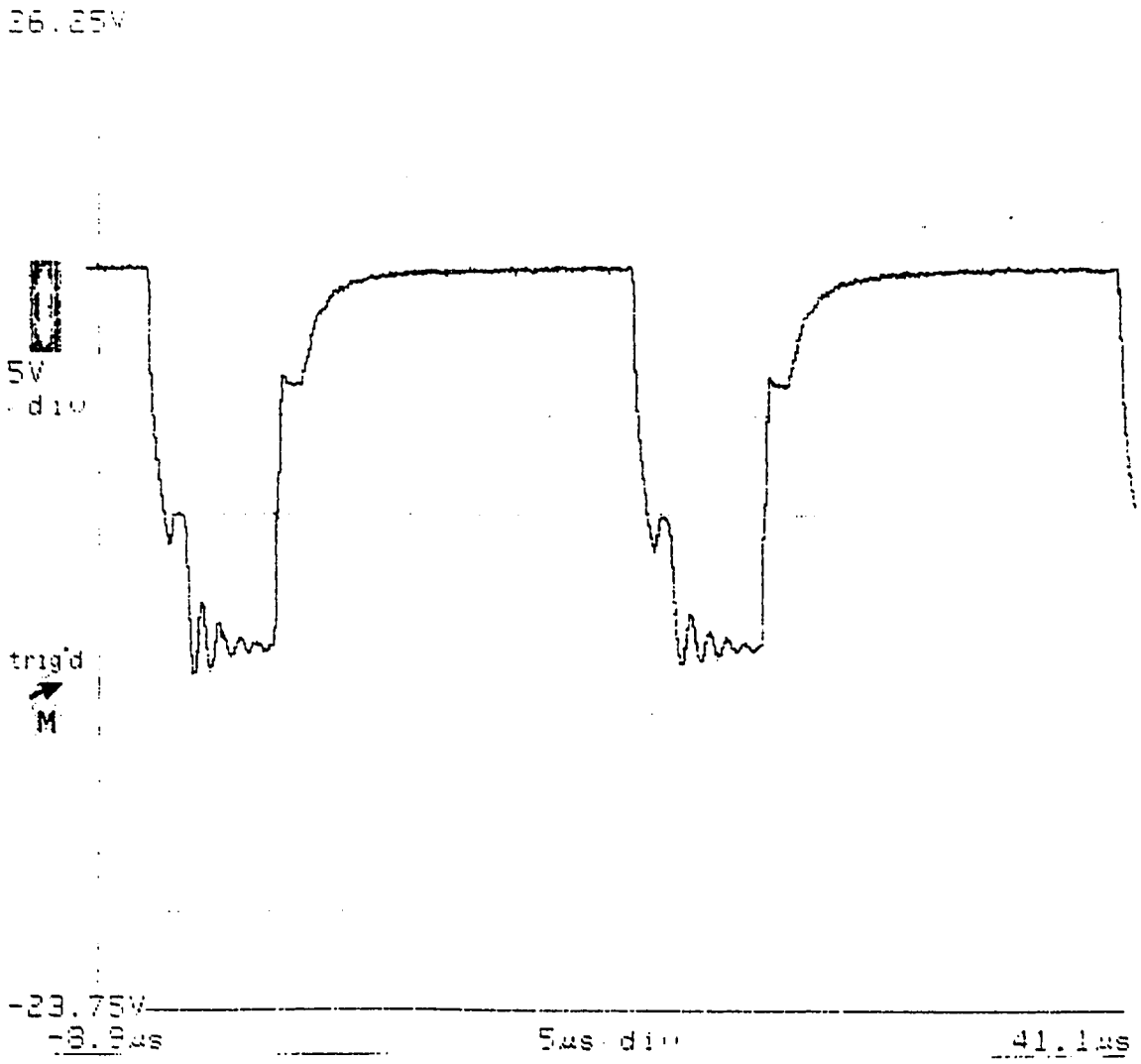


Figure D-4: Gating signal across the second transistor, T4, in the output bi-directional switch, S2, at 10 VAC at a minimum duty cycle of 0.25.

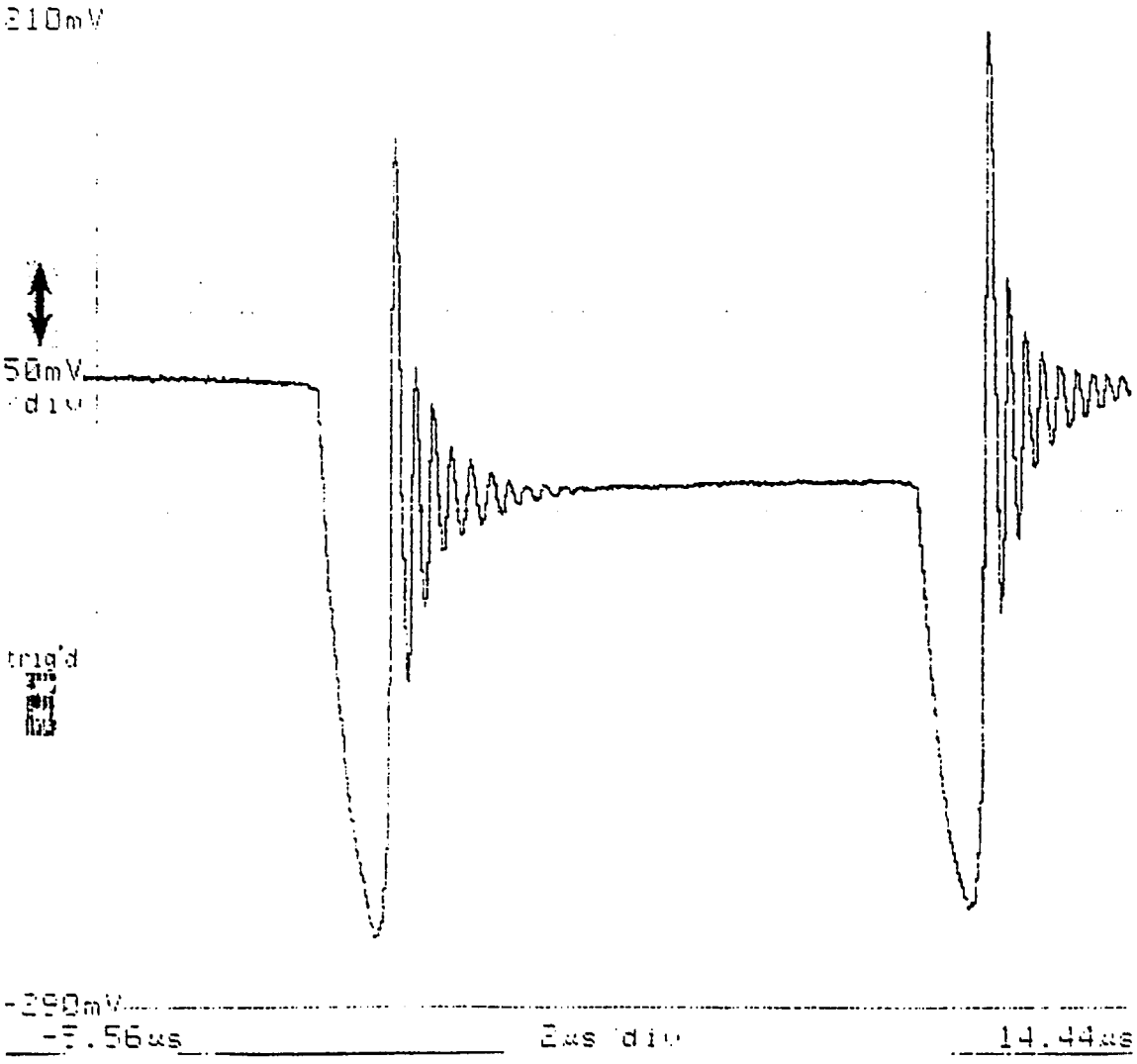


Figure D-5: Output current waveform (zoomed-in frequency range).

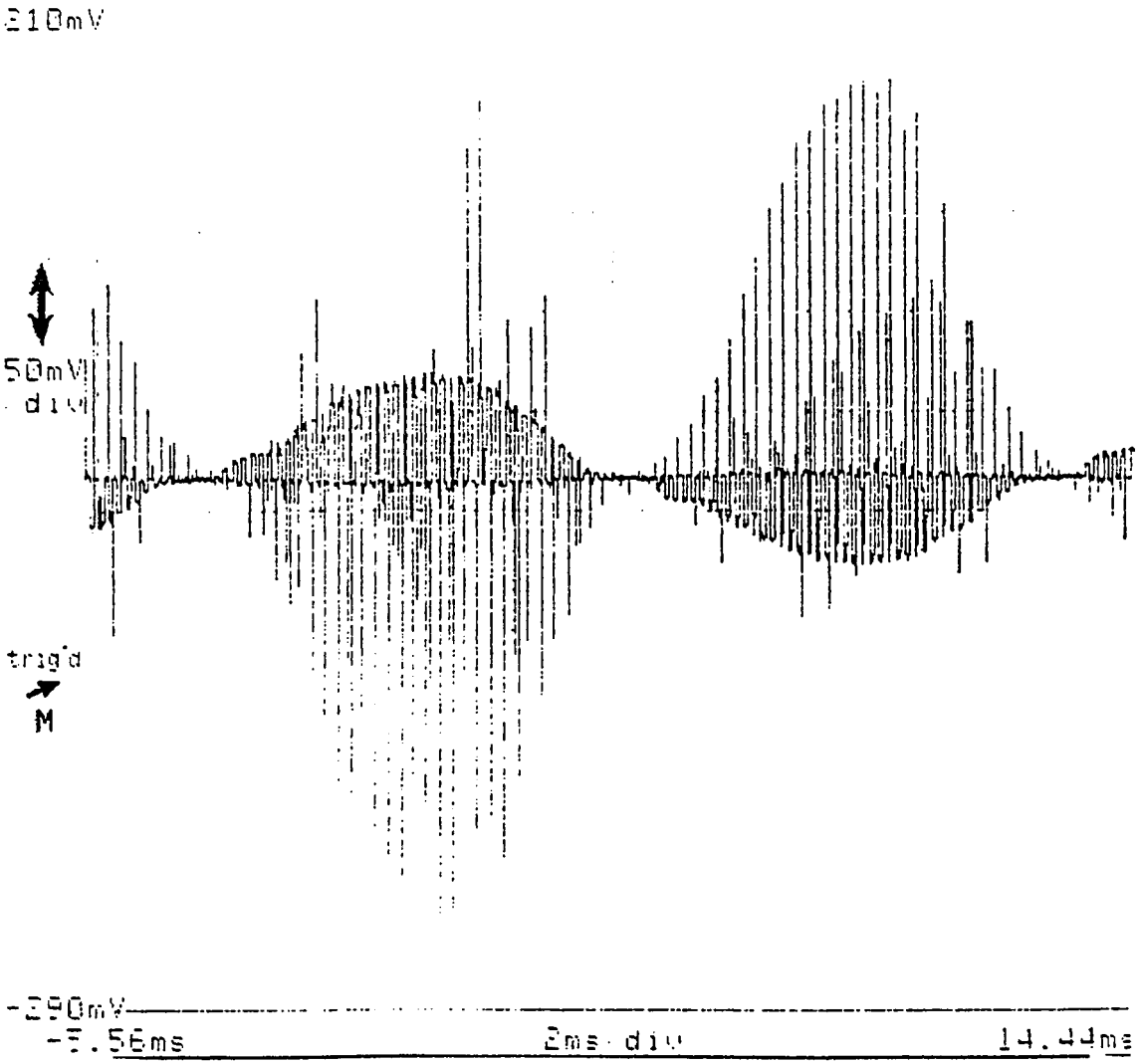


Figure D-6: Output current waveform (zoomed-out frequency range).

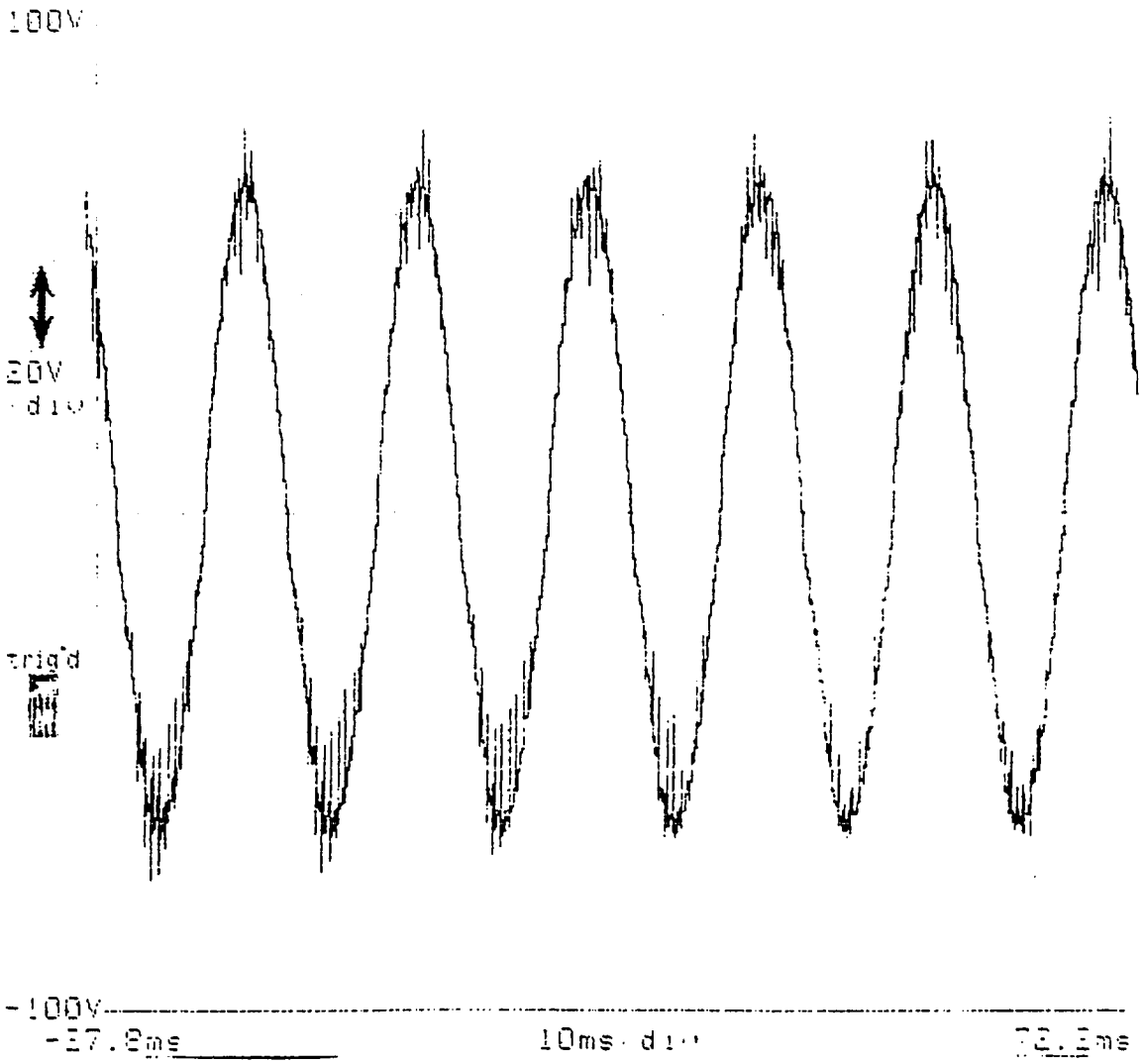


Figure D-7: Output voltage of 50 VAC into 100 watt light bulb.

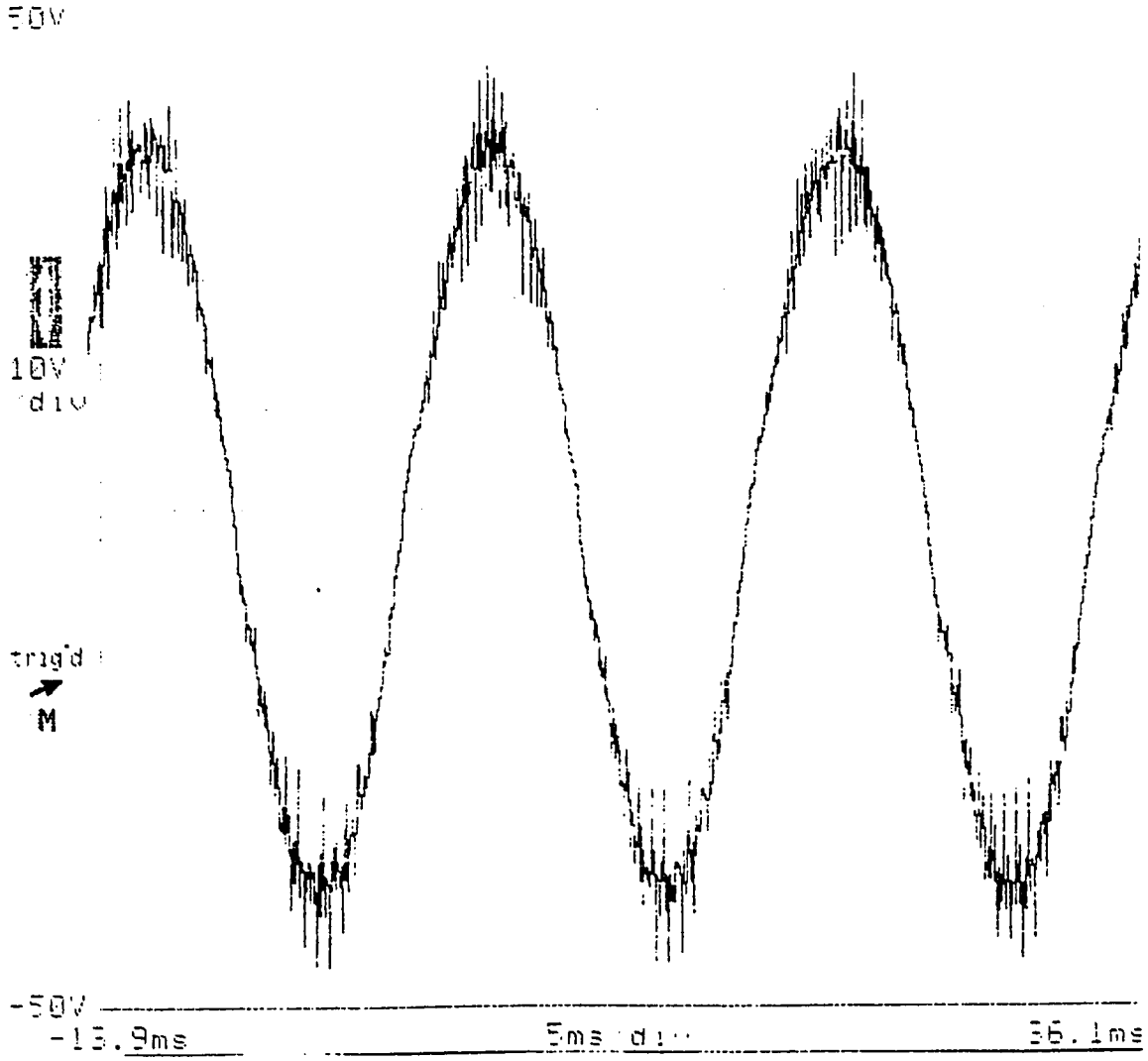


Figure D-8: Output voltage of 30 VAC into 100 watt light bulb.

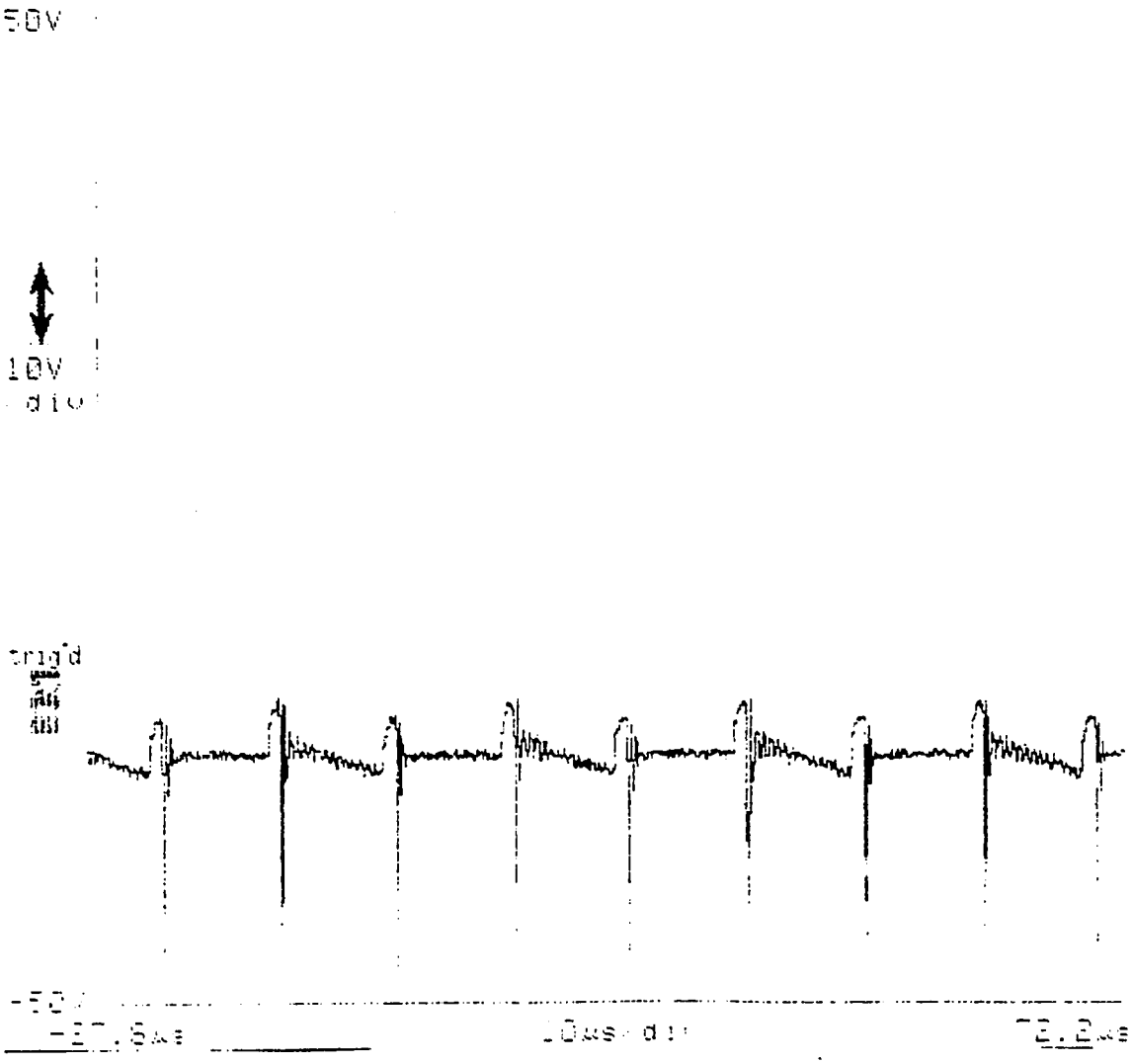


Figure D-9: Output voltage of 30 VDC into 100 watt light bulb without additional 4 × 0.47μ F capacitors (notice the large spikes).

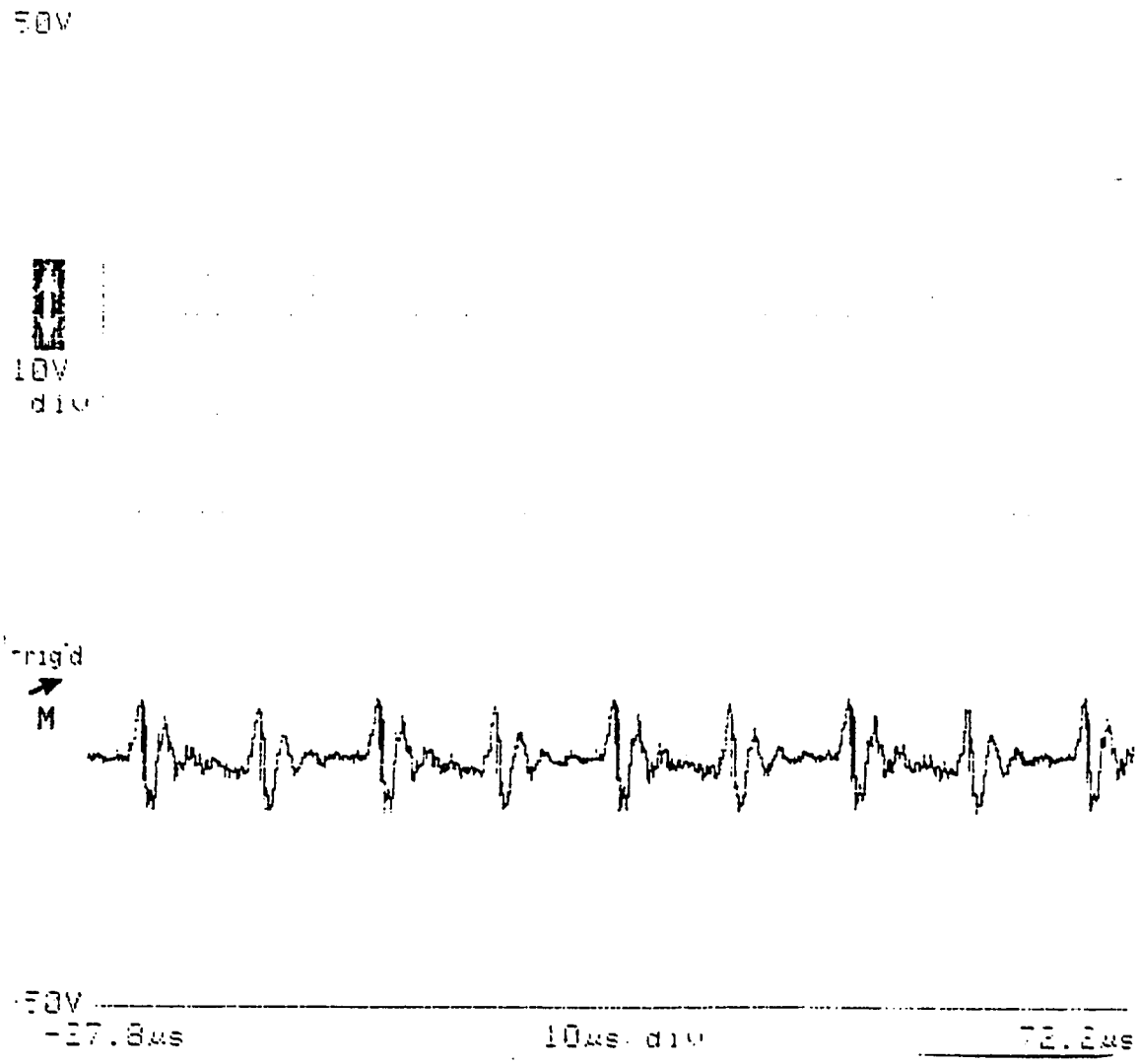


Figure D-10: Output voltage of 30 VDC into 100 watt light bulb with additional 4× 0.47μ F capacitors (notice the large spikes are eliminated).

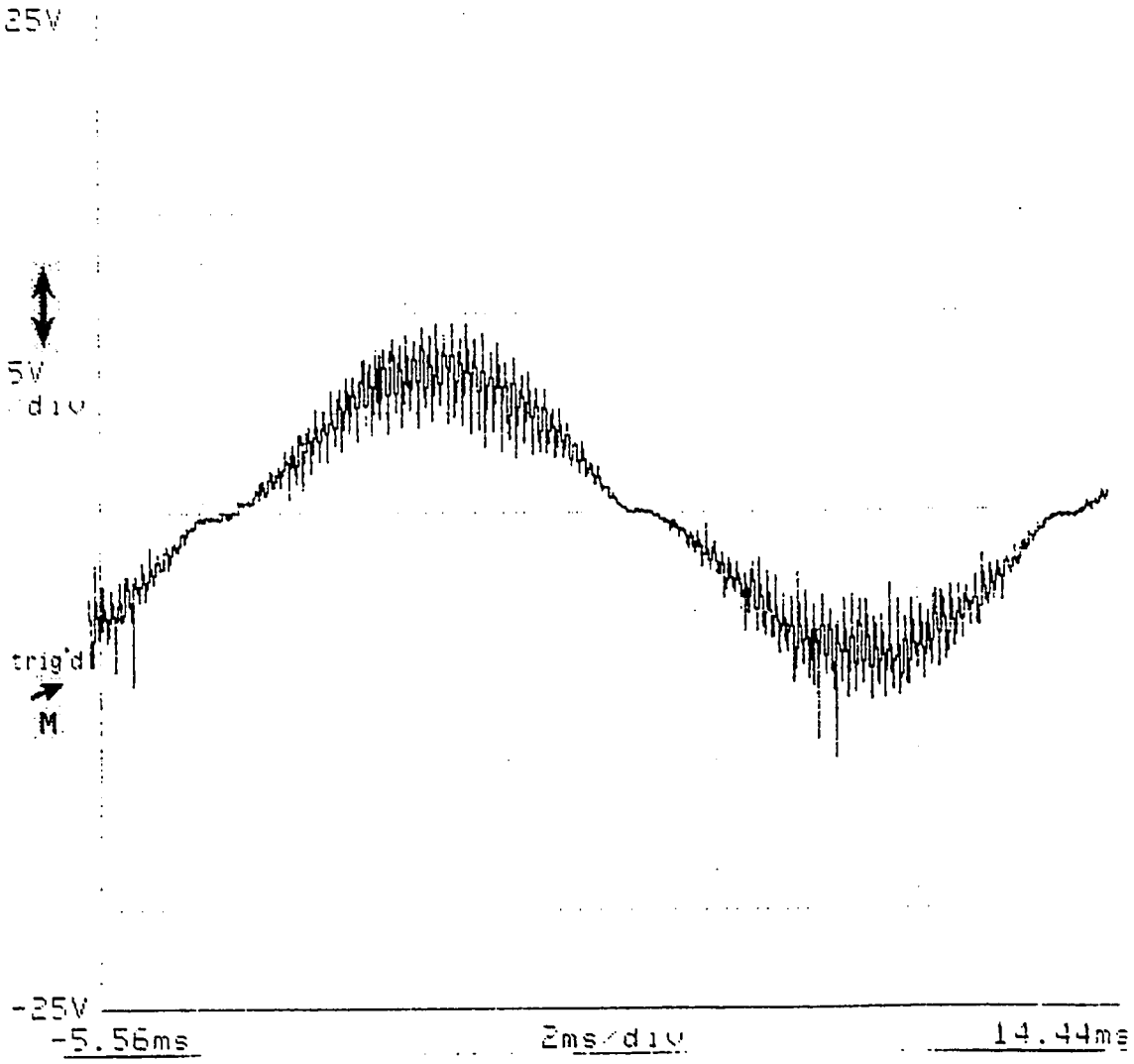


Figure D-11: Output voltage of 12 VAC into 100 watt light bulb without additional 4× 0.47μF capacitors (notice the large spikes).

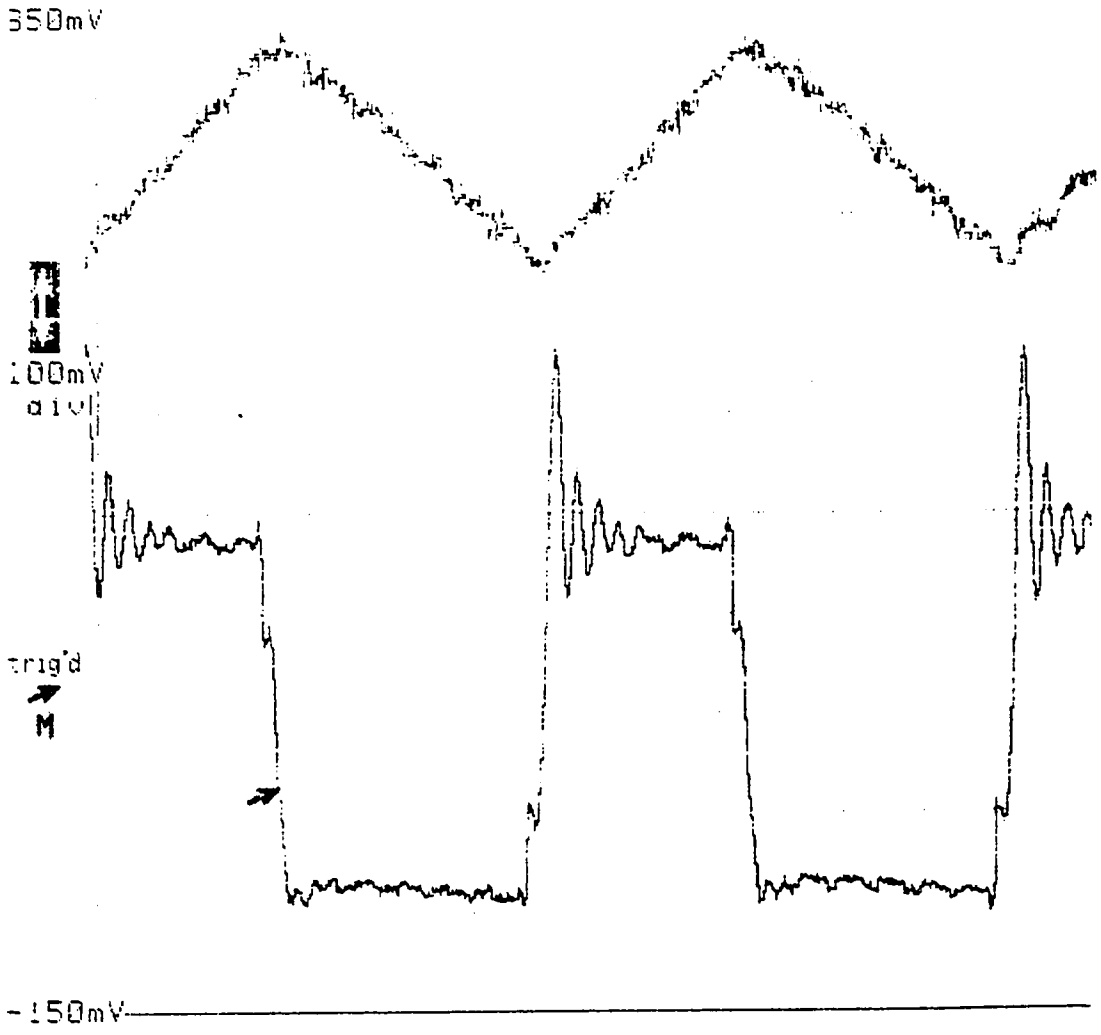


Figure D-12: Inductor current and voltage.

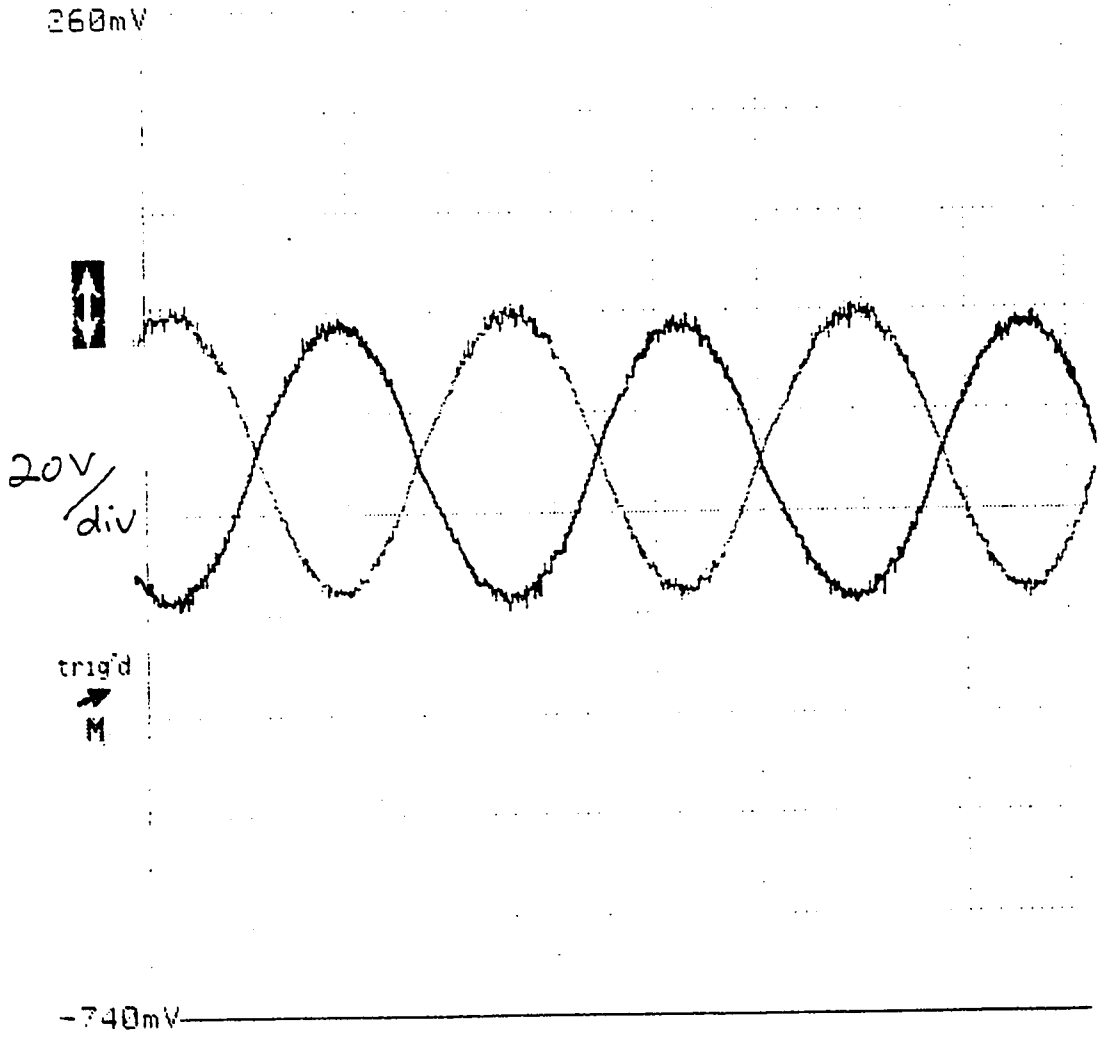


Figure D-13: V_o and V_{IN} no buck or boost operation of the converter at D = 0.5 measured across a 1 kΩ load $\left(V_O = \frac{D}{1-D} V_{IN} = \frac{0.5}{1-0.5} V_{IN} = V_{IN}\right)$.

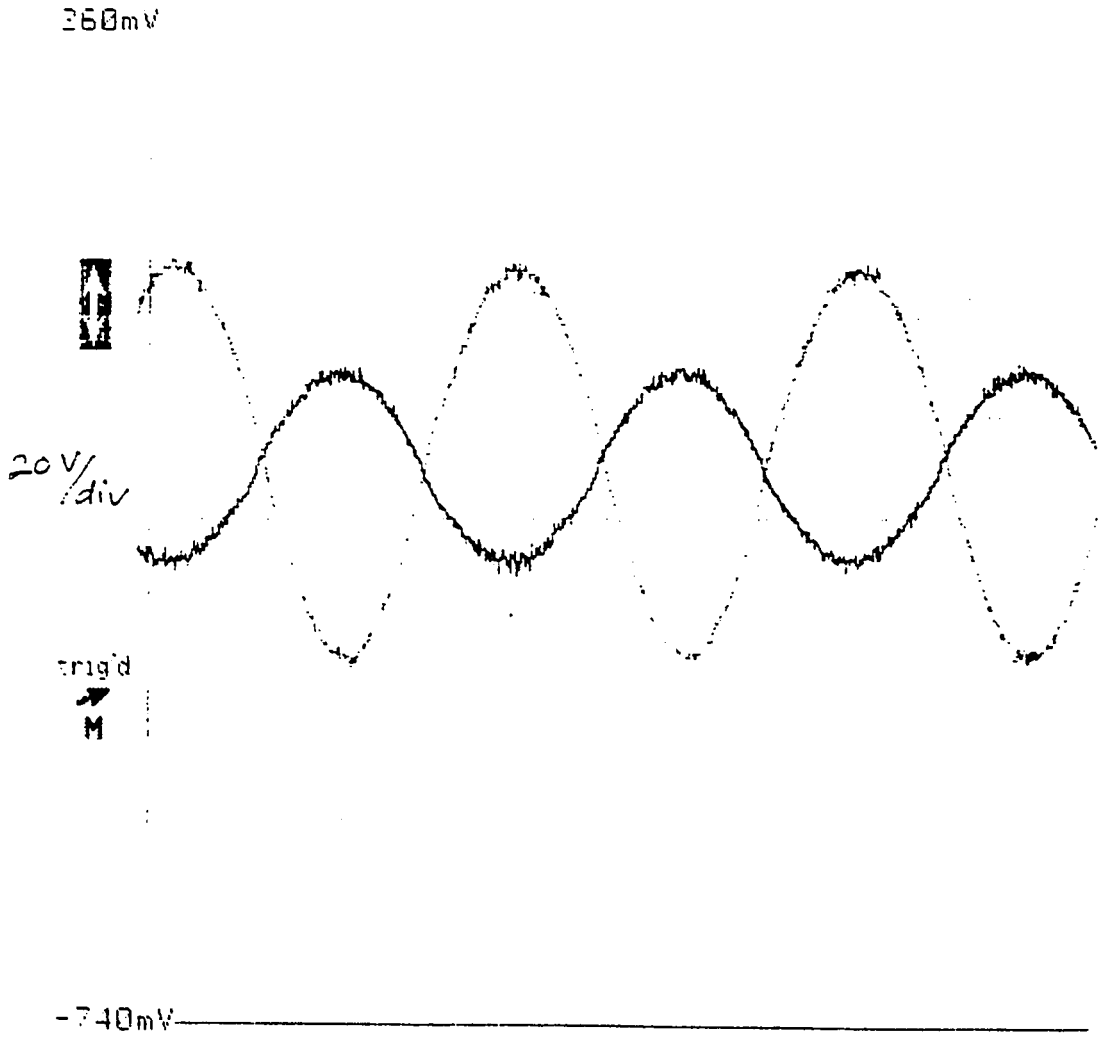


Figure D-14: V_o and V_{IN} boost operation of the converter at D = 0.75 measured across a 1 kΩ load

$$\left(V_O = \frac{D}{1-D} V_{IN} = \frac{0.75}{1-0.75} V_{IN} = 3 * V_{IN}\right)$$

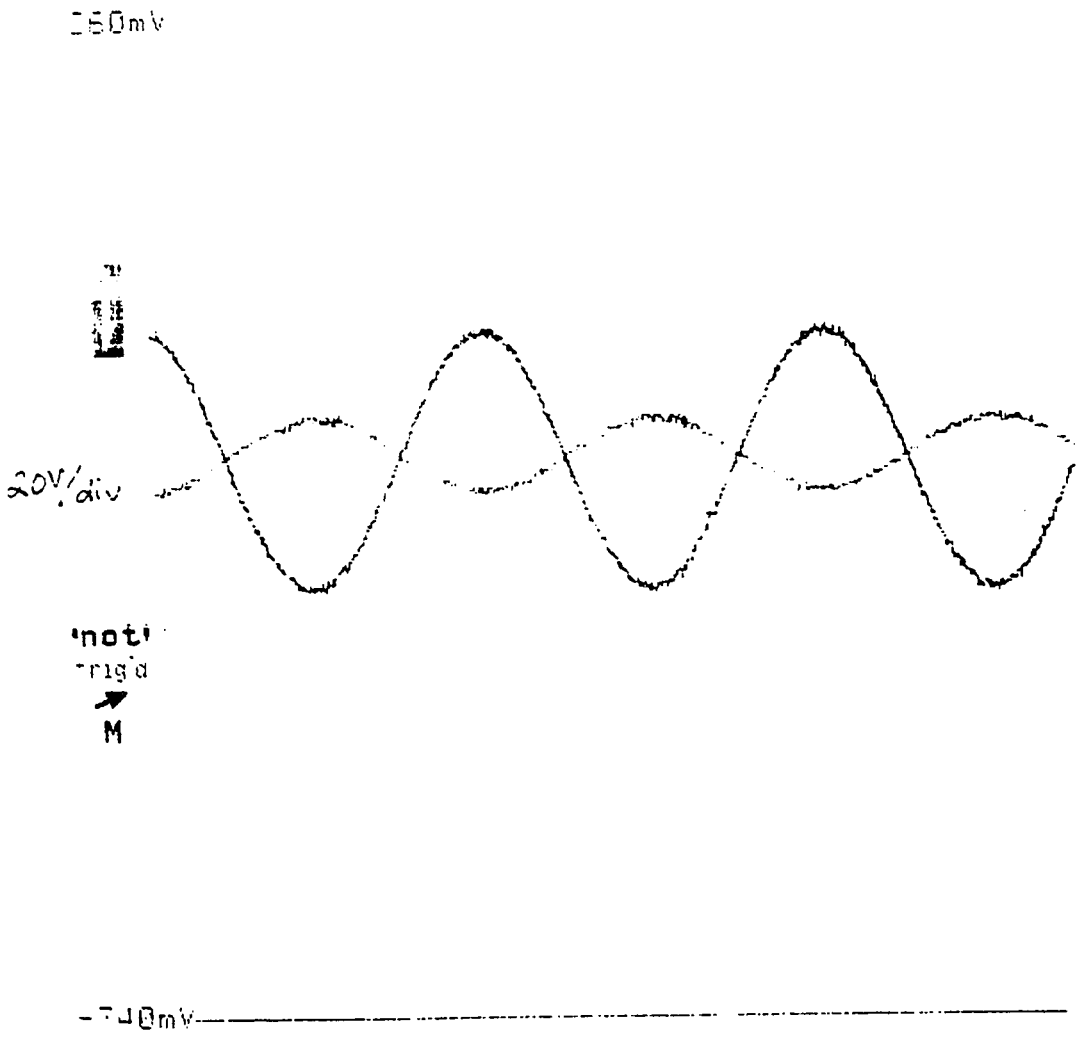


Figure D-15: V_o and V_{IN} buck operation of the converter at D = 0.25 measured across a 1 kΩ load

$$\left(V_O = \frac{D}{1-D}V_{IN} = \frac{0.25}{1-0.25}V_{IN} = \frac{V_{IN}}{3}\right).$$

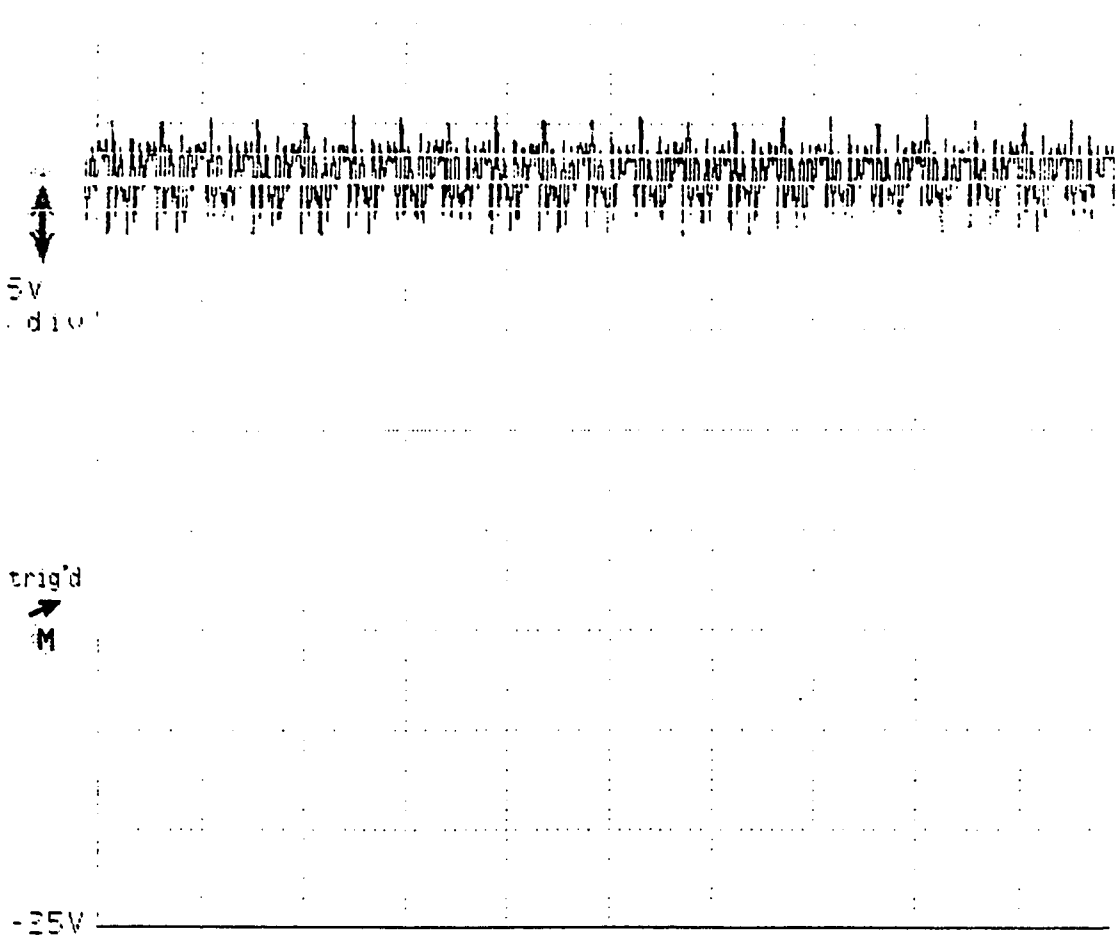


Figure D-16: Output voltage standard switching (bi-polar switching with all devices switching). Notice the spikes on the output.

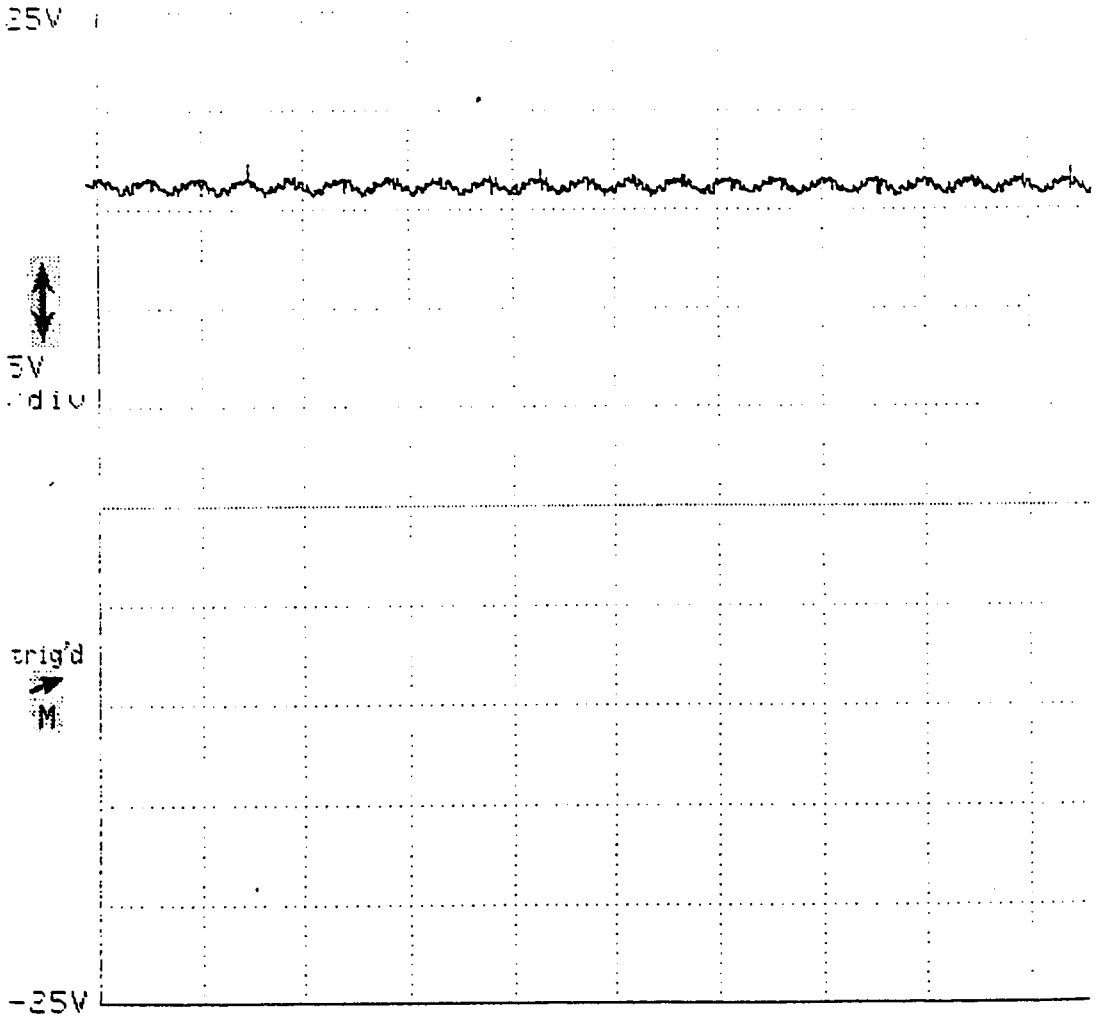


Figure D-17: Output voltage alternate switching (unipolar switching). Notice no spikes on the output.

APPENDIX E

MATLAB LISTING AND BODE PLOT RESULTS

This appendix presents :

1. Matlab listing for the program used to generate the bode plots. The listing includes model development for the direct duty cycle controlled system, the compensator design using the K-factor method, and the compensated system.
2. Bode plots of the:
    a. Compensator used to stabilize the system.
    b. System at one of the extremes of operation (compensated and uncompensated).
    c. System at another extreme of operation (compensated and uncompensated).
3. The two extremes are:
    a. Duty cycle = 0.25 and the output resistance was varied from 10 Ω to 1000 Ω. Both compensated and uncompensated systems were plotted. The gain of the system was 100, which is representative of $\frac{V_{IN}}{(1-d)^2} = \frac{40}{(1-0.25)^2} = 71.11$.
    b. Duty cycle = 0.75 and the output resistance was varied from 250 Ω to 1000 Ω. Both compensated and uncompensated systems were plotted. The gain of the system was 6000, which is representative of $\frac{V_{IN}}{(1-d)^2} = \frac{360}{(1-0.75)^2} = 5760$.

```
%***************************************
function [] = varsys(gain,boost,Wc,Rc,d,r)
% first parameteris the gain of the converter Vin/(1-D)^2
% second parameter is the required boost as described in K-factor method
% Boost = desired PM - modulator phase shift -90
% Wc is the desired cutoff frequancy
% Rc is the ESR of the filter capacitor.
% d is the duty cycle
% r is the output resistance
% in matlab multiply by 2*pi*frequency
% Example of the call to this matlab function
% varsys4(5760,(8/9)*pi,5e3,0,.75,1000)
%*********************************
%       buck boost design
% K factor calculation
k = (tan((boost/4)+(pi/4)))^2;
%*********************************
% capacitor value
c = 25e-6;
%*********************************
% inductor value
l = 133e-6;
%*********************************
% resonant frequancy
Wo = (1-d)/((l*c)^.5);
b = 1/(1-d)^2;
Q = r /(Wo*l);
%*********************************
% He denominator
hd = [(1/Wo)^2 1/(Wo*Q) 1];
%*********************************
% ESR zero
nz = [(Rc*c) 1];
%*********************************
% nominator of system
nums = b * [-(d*l)*b/r 1];
nums = gain * conv(nums,nz);
%*********************************
% denominator of system
dens = hd;
```

Figure E-1: Matlab program listing.

```
%*********************************
% calcualte gain of system at cross over frequancy
a1= polyval(nums,Wc*2*pi);
a2= polyval(dens,Wc*2*pi);
aa1 = a1/a2;
%pzmap(nums,dens);
%pause
%printsys(nums,dens)
roots(nums);
roots(dens);
w = (1:1000:1e7);
%[mag,phase,w] = bode(nums,dens);
%[gm,pm,wcg,wcp]= margin(mag,phase,w);
%pm
%wcp
bode(nums,dens,w);
pause
%*********************************
% compensator two zeros at Wo and three poles one at origin and two to compensate
%for the RHP zero and the ESR zero
% This is just following the K-factor method which states that
% the two zeros should be at f/sqrt(k), the two poles at f*sqrt(k)
Wz = Wc/(k)^(0.5);
Wp = Wc*(k)^(0.5);
%*********************************
% nominator of the compensator
nz1 = [1/(2*pi*Wz) 1];
nz2 = nz1;
nc =  conv(nz1,nz2);
%*********************************
% denominator of the compensator
dp1 = [1 1];
dp2 = [1/(2*pi*Wp) 1];
dp3 = [1/(2*pi*Wp) 1];
dc1 = conv(dp1,dp2);
dc = conv(dc1,dp3);
%*********************************
% gain of the compensator at the cross over frequancy
% should be equal to 1/(gain of the modulator at the cross over frequancy
a1= polyval(nc,Wc*2*pi);
a2= polyval(dc,Wc*2*pi);
```

Figure E-1 (continued): Matlab program listing.

```
aa2 = a1/a2;
gainc = 1/(aa1*aa2);
%*********************************
% recalculate nominator of the compensator
nc = gainc * nc;
%pzmap(nc,dc)
%pause
%bode(nc,dc);
%pause
%*********************************
% nominator and denominator of the compensated system
numcs = conv(nums,nc);
dencs = conv(dens,dc);
%*********************************
% calculate dc gain of the system
dcgain(numcs,dencs);
%*********************************
% plot the bode plot of the system
% calculate the Phase margin and gain margin
% and WCP= gain cross over frequancy
% and WCG= phase cross over frequancy
%*********************************
bode(numcs,dencs);
[mag,phase,w] = bode(numcs,dencs);
[gm,pm,wcg,wcp]= margin(mag,phase,w);
pm
gm=20*log10(gm)
wcg
wcp
```

Figure E-1 (concluded): Matlab program listing.

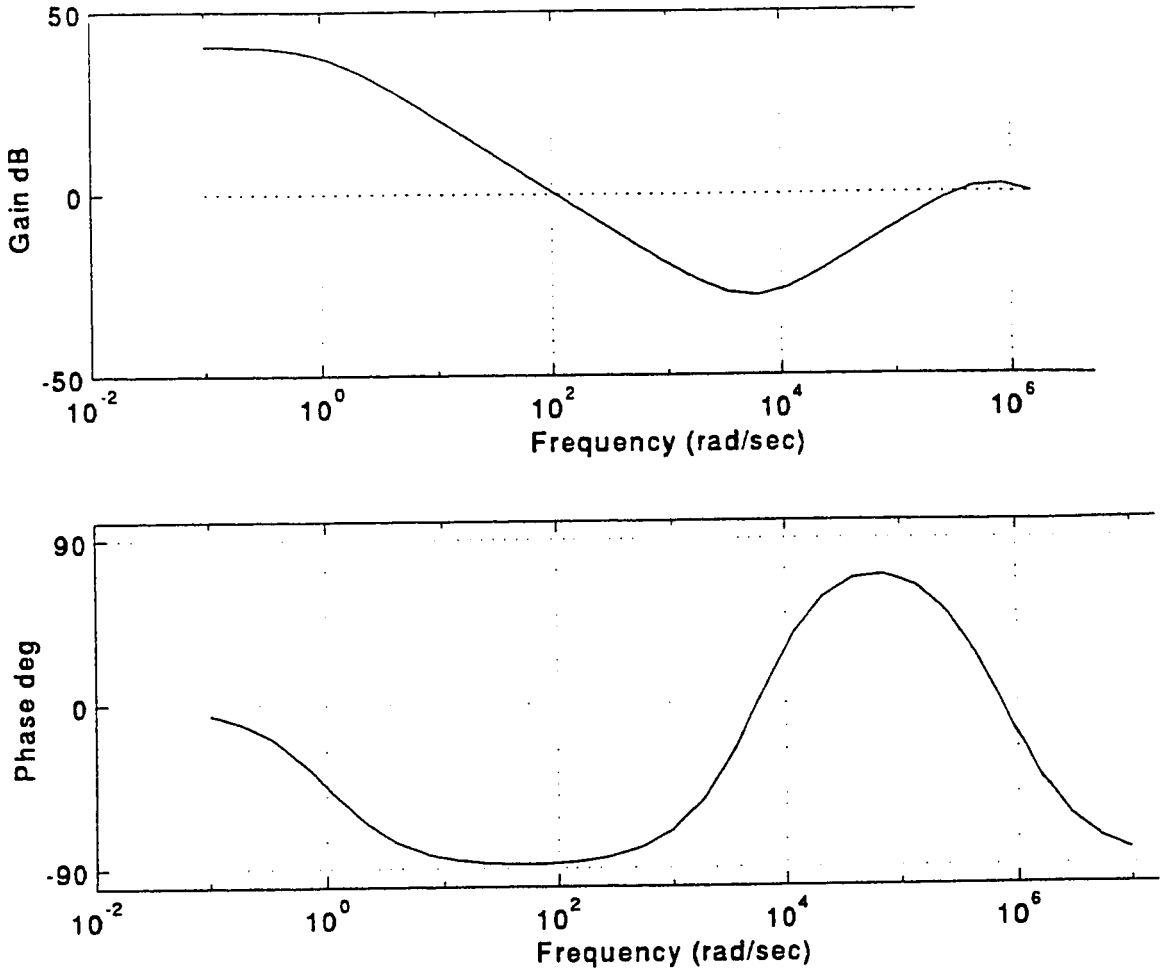


Figure E-2: Bode plot of compensator. Two-zero three-pole compensator; boost = 160 deg.

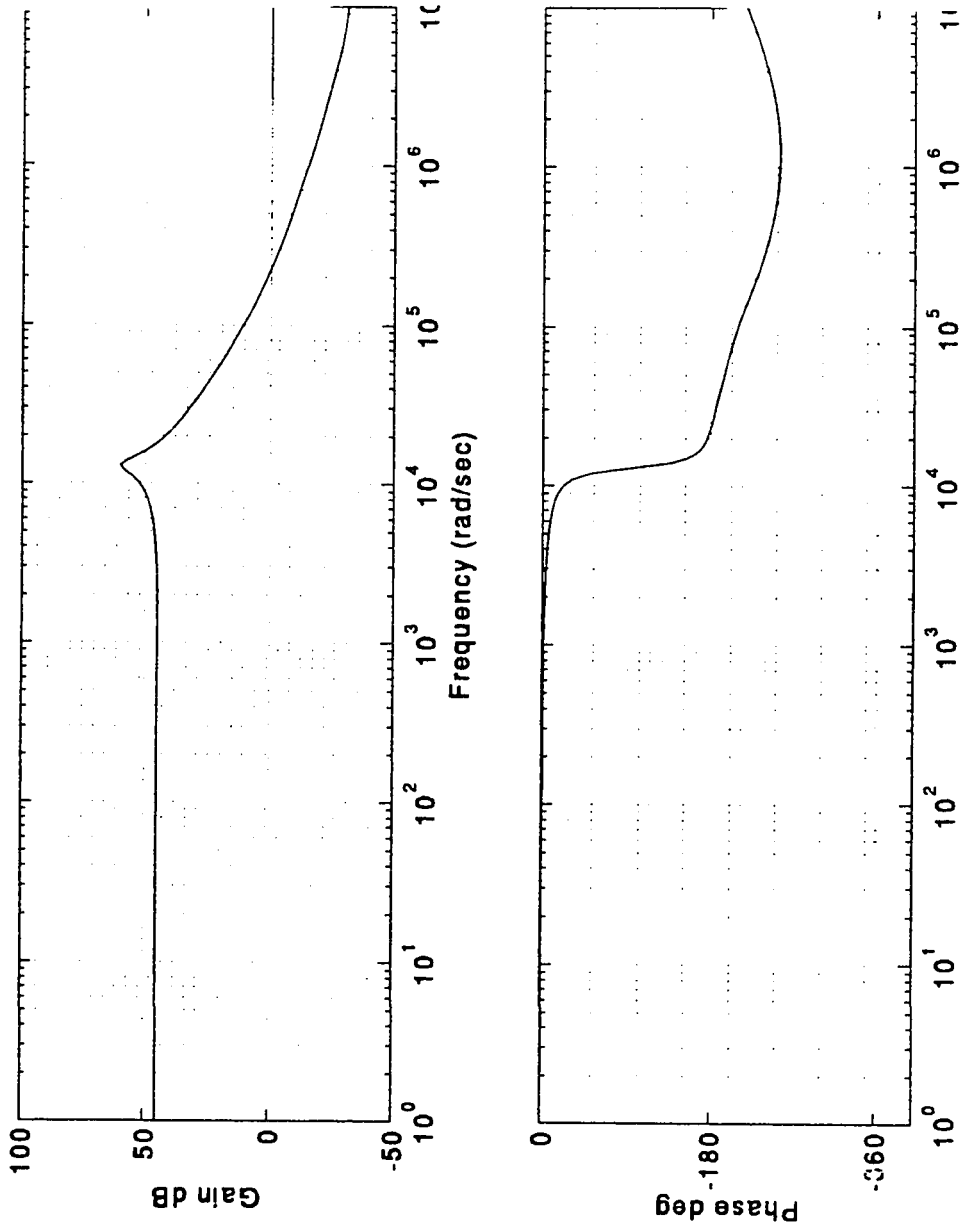


Figure E-3: Bode plot of uncompensated system; gain = 100, R_C = 5 mΩ R = 10 Ω D = 0.25.

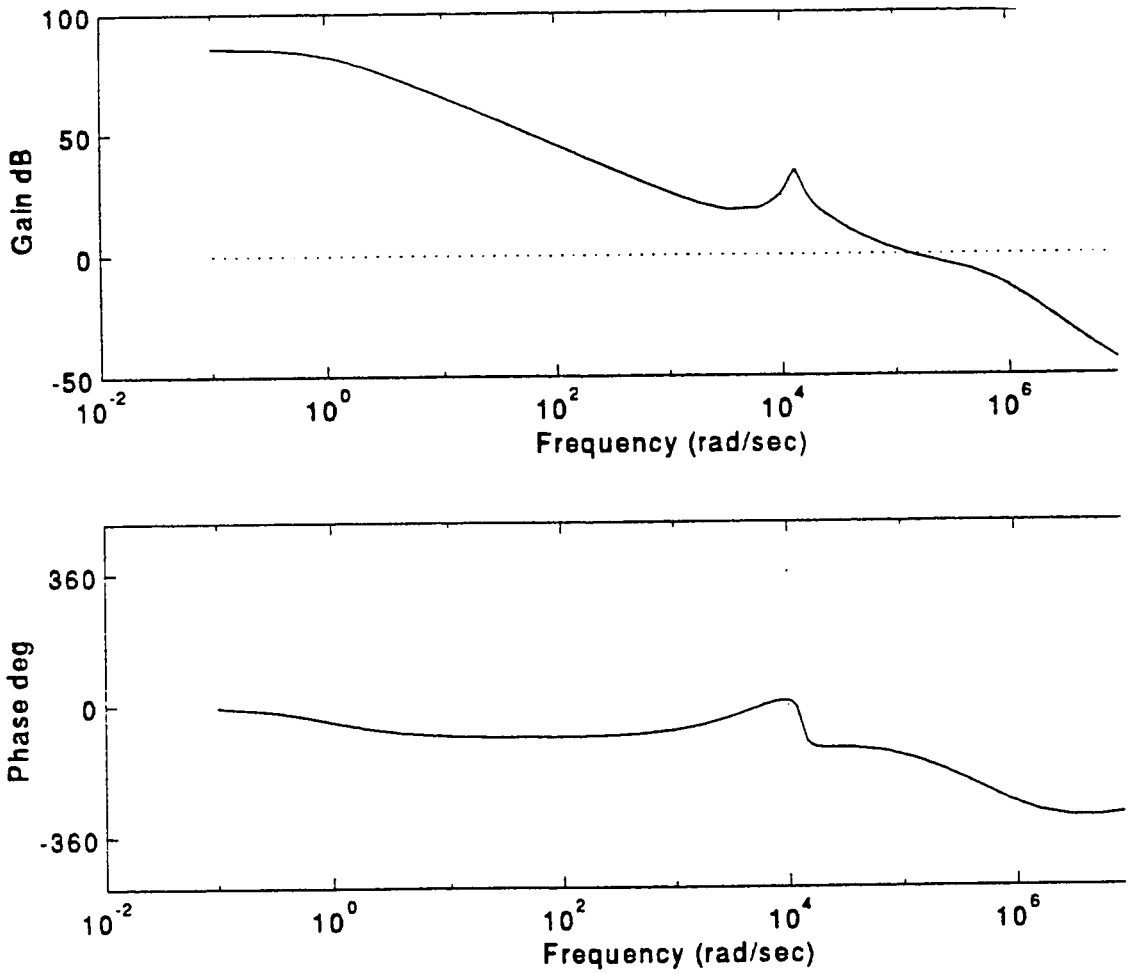


Figure E-4: Bode plot of compensated system; gain = 100, R_C = 5 mΩ, R = 10 Ω, D = 0.25, phase margin = 27.7, gain margin = 2.8464, W_{CG} = 2.29e5 rad/sec, and W_{CP} = 1.3349e5 rad/sec (where W_{CG} is the phase crossover frequency and W_{CP} is the gain crossover frequency).

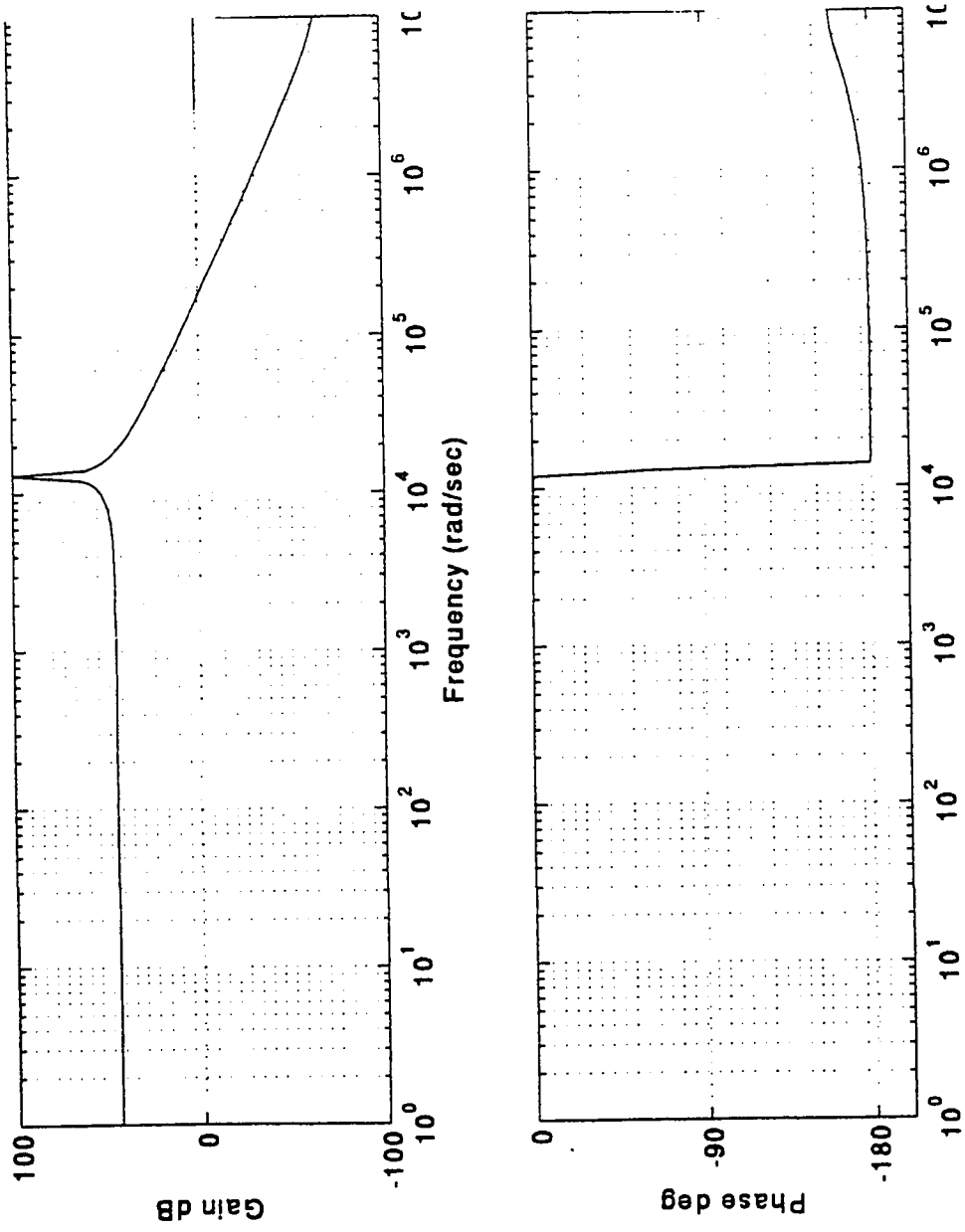


Figure E-5: Bode plot of uncompensated system; gain = 100, R_C = 5 mΩ, R = 1000 Ω, D = 0.25.

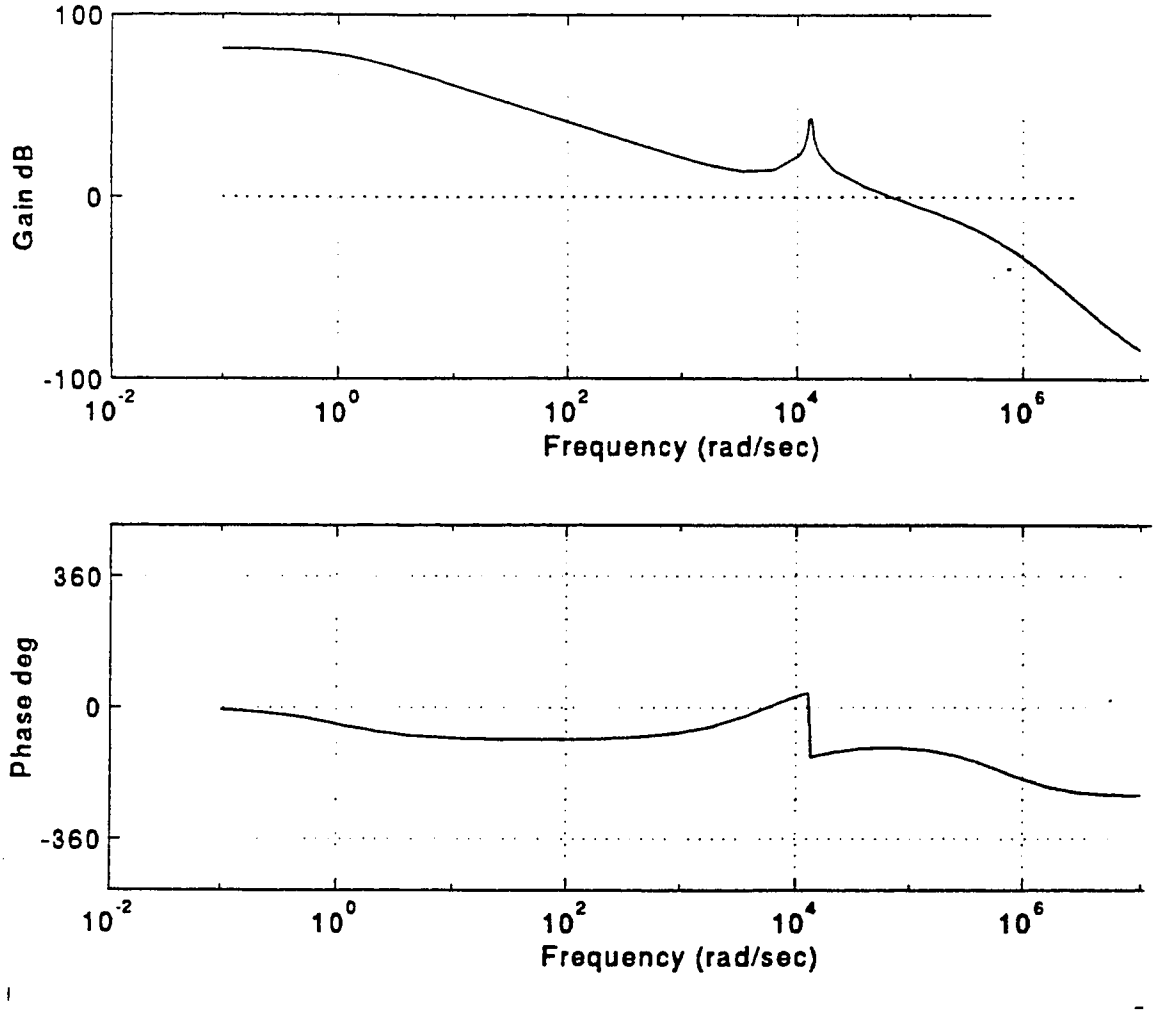


Figure E-6: Bode plot of compensated system; gain = 100, R_C = 5 mΩ, R = 1000 Ω, D = 0.25, phase margin = 69.8, gain margin = 27.65, W_{CG} = 67950 rad/sec, and W_{CP} = 741750 rad/sec sec (where W_{CG} is the phase crossover frequency and W_{CP} is the gain crossover frequency).

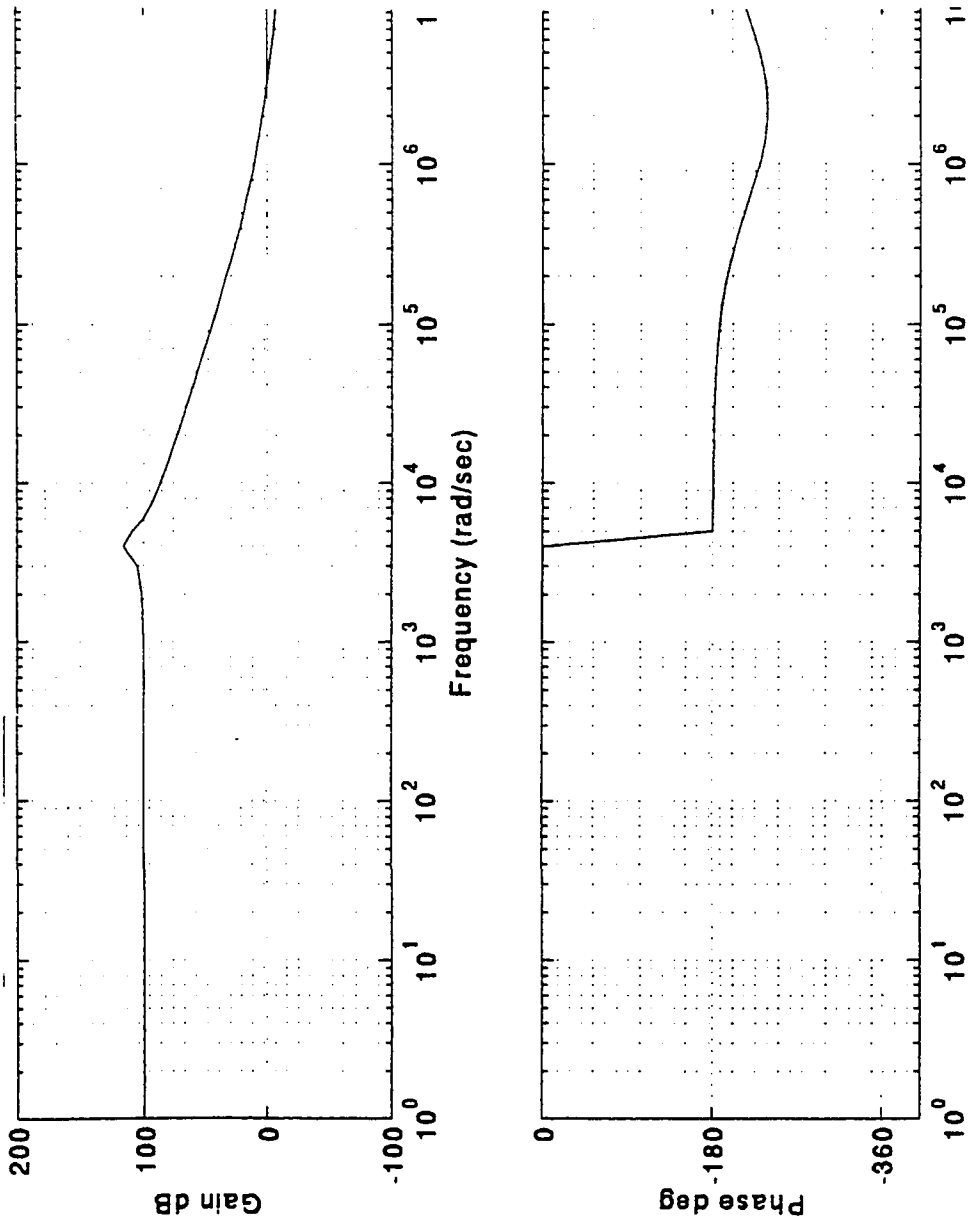


Figure E-7: Bode plot of uncompensated system; gain = 6000, R_C = 5 mΩ, R = 1000 Ω, d = 0.75.

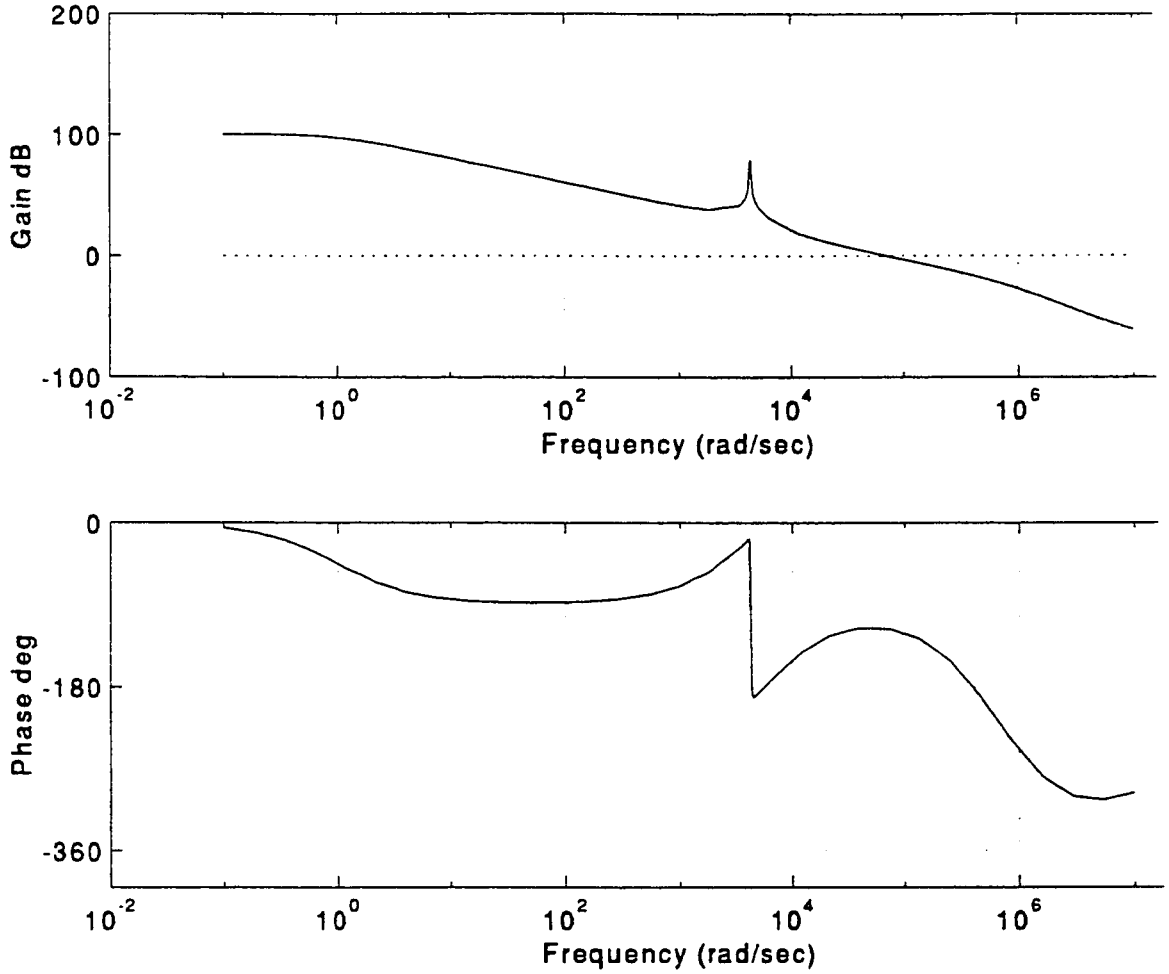


Figure E-8: Bode plot of compensated system; gain = 6000, R_C = 5 mΩ, R = 1000 Ω, D = 0.75, phase margin = 63.66, gain margin = 15.98, W_{CG} = 7.014E4 rad/sec, and W_{CP} = 3.9491E5 rad/sec (where W_{CG} is the phase crossover frequency and W_{CP} is the gain crossover frequency).

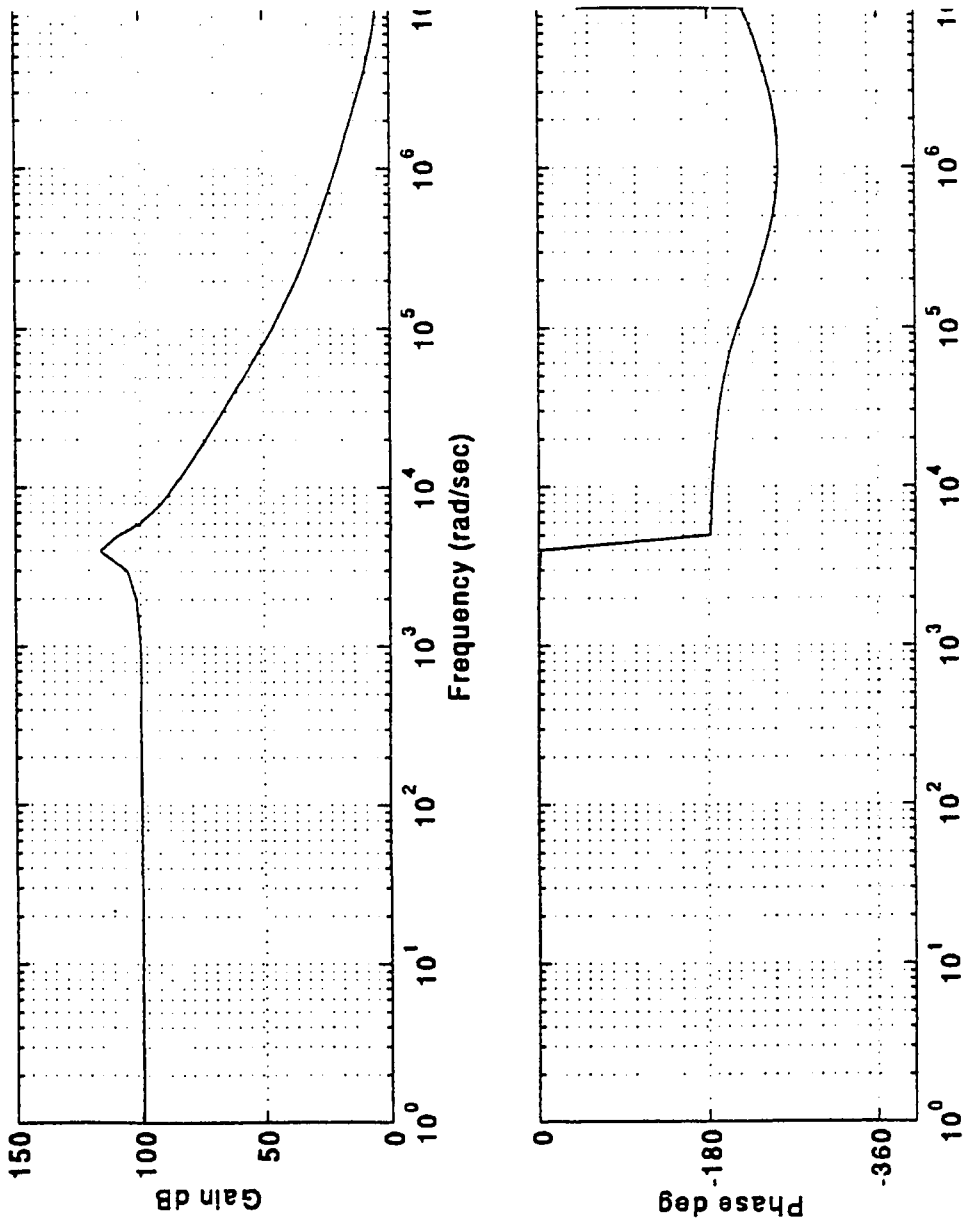


Figure E-9: Bode plot of uncompensated system; gain = 6000, R_C = 5 mΩ R = 250 Ω d = 0.75.

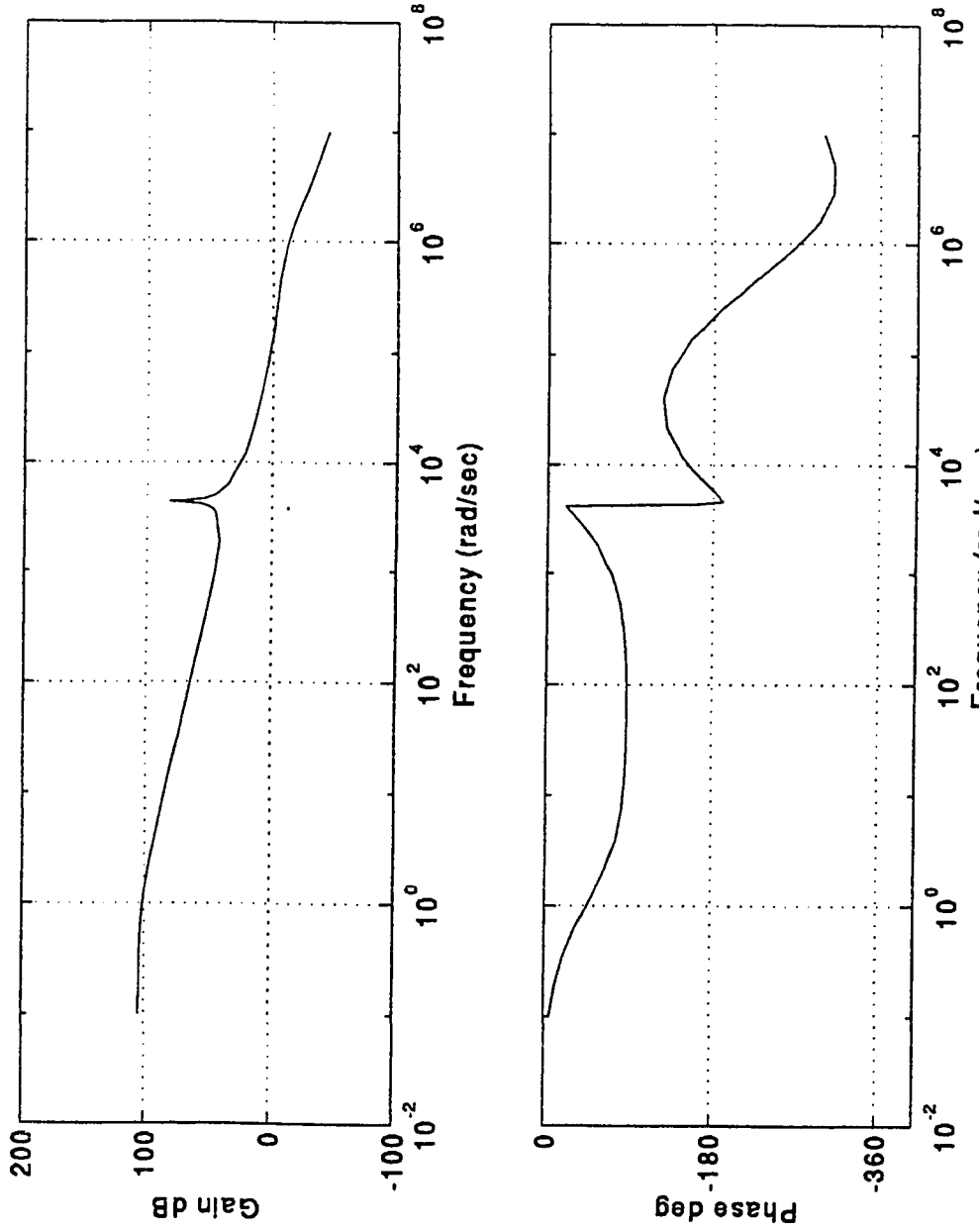


Figure E-10: Bode plot of compensated system; gain = 6000, R_C = 5 mΩ, R = 250 Ω, D = 0.75, phase margin = 24.58, gain margin = 2.38, W_{CG} = 133500 rad/sec, and W_{CP} = 217590 rad/sec (where W_{CG} is the phase crossover frequency and W_{CP} is the gain crossover frequency).